Design and performance of the ALICE TRD frontend electronics

- Introduction
- Multi Chip Module - PASA+TRAP
- Readout tree and GTU
- TRAP and MCM production test
- Conclusions

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TRD Structure

- 1.2 million channels
- 1.4 million ADCs
- peak data rate: 16 TB/s
- ~65000 MCMs
- computing time: 6 µs

TR-detector

- 18 sectors in azimuth
- 5 module rings
- 6 planes
- 18 channels
- 1.2 million channels
- 1.4 million ADCs
- peak data rate: 16 TB/s
- ~65000 MCMs
- computing time: 6 µs

module

MCM

chamber

- 8 MCM = 144 channels

MCM performs amplification, digitization, straight line fit, readout network
TRD & MCM Functionality

**TRD chamber**
- The TRD is a drift chamber to detect the trajectory of charged particles.
- In addition, a radiator stack in front to cause transition radiation to separate electrons from pions.

**Multi Chip Module**
- The MCM amplifies and digitizes the analog signals and stores the data.
- It performs a line fit and ships the track data off the detector to a global tracking unit.
- Sends zero-suppressed ADC data after L1A.

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**Transition Radiation Detector**
- The TRD is a drift chamber to detect the trajectory of charged particles.
- In addition, a radiator stack in front to cause transition radiation to separate electrons from pions.

**Event display for MCM functionality**
Line Fit & Global Tracking

**tracklet processor**
- straight line fit via a linear regression method
- searching for dedicated patterns (for energy cut and electron - pion separation)
- raw data buffer

**global tracking**
- projection of ‘tracklets’ to a virtual plane
- searching for tracklets belonging together
- perform cut and generate trigger
Data Flow and Data Reduction

MCM - Multi Chip Module

- TRD
- PASA
- ADC
- Tracklet Preprocessor TPP
- Tracklet Processor TP
- Network Interface NI
- GTU
- L1 trigger to CTP
- to HLT & DAQ

- Event buffer
  store raw data until L1A

- Detector
  6 layers
  1.2 million analog channels
- Charge sensitive preamplifier shaper
- 10 Bit ADC
  10 MSPS
  21 channels
- Digital filter
  preprocess data
  event buffer
- Fit tracklets for trigger functionality
  process raw data
  monitoring
- Builds readout tree
  for trigger & raw data
- Merge tracklets into tracks for trigger
  process raw data for HLT

- Time:
  - during first 2 µs (drift time)
  - after 3.5 µs
  - after 4.1 µs
  - after 6 µs

- Data / event:
  - 33 MB
  - 16 TB/s
  - max. 80 KB
  - ~ 400

- Peak rate:
  - 257 GB/s
  - 600 GB/s
  - -
  - to trigger decision

- Mean rate:
  - 1
  - -
  - ~ 400

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Multi Chip Module

PASA

Internal ADCs (Kaiserslautern)

Digital Frontend and Tracklet Preprocessor

MIMD Processor:
- 4 CPUs,
- Global Register File,
- Interrupt controllers,
- Counter/Timers,
- Arbiter for the Global I/O Bus

Master State Machine

Network Interface

Serial Interface slave

External Pretrigger

Serial Interface

Readout Network

Instrution Memory

Quad-ported DMEM

Global I/O-Bus

4 cm
PASA - Preamplifier and Shaper

PASA - Preamplifier and Shaping Amplifier
- FWHM: 116 ns
- ENC: 850 electrons at 25 pF
- Gain: 12 mV/fC
- Integral Nonlinearity: 0.3%
- Power: 3.3V, 90 mA / chip
- Process: 0.35µm AMS
- Area: 21.3 mm²
- Yield: 99.8% of the first 20 000 chips
ADC - Analog to Digital Converter

functionality of cyclic ADCs

ADC - Analog to Digital Converter
Prof. Tielert, Uni Kaiserslautern
♦ 10 Bit, 10 MSPS, no latency
♦ Cyclic ADC, 240 MHz internal
♦ ENOB: 9.5
♦ Power: 10 mW / channel (programmable)
♦ Area: 0.11 mm² (550 x 200 µm²)
Sinwave measured using one CPU to copy the ADC data into the memory.

Note that by the normal operation in the detector the ADC data will be processed and stored without turning on the CPUs.
Filter & Preprocessor

Filter & event buffer
- history fifo
- nonlinearity corr.
- pedestal corr.
- gain adjustment
- tail cancellation
crosstalk cancel.
event buffer

Preprocessor
- channel selection
- position calculation
- position correction
- max. 4 position
- calculate sums for regression
- select candidates

21 digital channels from ADCs (10 MHz)

21x

channel selection

position calculation

position correction

max. 4 position

calculate sums for regression

select candidates

232

to processor

ADC values
Nonlinearity
Tail Cancellation
Crosstalk Cancellation

amp

deflection
time bins

origin

COG

L

C

R

y-1

y

y+1

pos

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MIMD Processor

MIMD processor
- 4 CPUs
- shared memory / register file
- global I/O bus arbiter
- separate instruction memory
- coupled data & control paths

CPU
- Harvard style architecture
- two stage pipeline
- 32 Bit data path
- register to register operations
- fast ALU
  - 32x32 multiplication
  - 64/32 radix-4 divider
- maskable interrupts
- synchronization mechanisms

Preprocessor, 4 sets of fit data
SCSN - Slow Control Serial Network

- Up to 126 slaves per ring
- CRC protected
- 24 MBit/s transfer rate
- 16 addr., 32 databits/frame
Readout Tree

~1.2 million analog channels

- 65664 signal processing MCMs
  - 3 to 1 trees
- 16416 data collecting and signal processing MCMs
  - 4 to 1 trees
- 4104 data collecting MCMs
  - 4 to 1 trees
- 1080 data collecting MCMs
  - direct connection

- 1080 x 2.4 GBit/s optical Links (OASE)
- optical fibers
- global tracking unit

NI - Network Interface

- I/O interfaces
  - direct access via local I/O interfaces
  - global I/O configuration and status registers
- 4 input, 1 output ports
  - 8 Bit data at 120 MHz DDR (240 MB/s)
  - strobe, parity and spare bit
- data resynchronization
- input fifos (256 Bytes / port)
- 1 clock cycle input to output latency incl. data resynchronization

Readout

- collecting data of 65664 MCMs
- interface to the GTU are 1080 optical links with 2.4 GBit/s each
- readout latency: ~200 ns
- full trigger readout within 600 ns
Detector Readout

- **Pretrigger**
  - 0

- **Drift time**
  - Preprocessing finished
  - 2

- **Processing time**
  - Resulting track segments are delivered to the NI, processor is switched off
  - 4

- **Transmission time**
  - GTU starts 200ns after processing (transfer), after 600ns all data is transferred
  - 4.6

- **GTU finished**
  - 6

**On-MCM signal processing**

- ~1,200,000 channels / ADCs
  - 10 Bit, 10 MSPS
  - 20 samples/event preprocessing

- ~65,000 MCMs
  - 18 channels/MCM
  - 4 CPUs at 120 MHz
  - 4 tracklets/MCM at max.

**Network Interface Readout**

- ~4,100 Readout Boards
  - 16+1 MCMs/board
  - 8 Bit data, 120 Mhz DDR collected via tree structure

**Optical transmission via OASE**

- 1,080 Optical Links (OASE)
  - 2 links/chamber
  - 2.4 GB/s, integrated serializer/deserializer

- 90 Track Matching Units (GTU)
  - 1 TMU/module
  - 2.4 GBit/s, integrated serializer/deserializer

- 1 Central Trigger Proc.
OASE - Optical Advanced SErializer
Prof. Brüning, Uni Mannheim
Prof. Tielert, Uni Kaiserslautern

♦ 8 Bit at 120 MHz DDR parallel ↔ 2.4 GBit/s serial transceiver
♦ SCSN and I²C configuration interfaces, JTAG
♦ pins to directly connect laser diodes for on-chip connection
Replacement for the OASE board with the same connector and speed
♦ 8 Bit at 120 MHz DDR parallel to 16 bit SDR 120 MHz conversion using CPLD
♦ Commercial gigabit serializer from Texas Instruments
♦ Driver for the laser diode

Receiver board for testing of the gigabit serializer board
♦ Amplifier for the photodiode
♦ Commercial gigabit deserializer from Texas Instruments

The main drawback of this solution is the higher price and the larger number of components
Global Tracking Unit
♦ receive data from 1080 optical links
♦ process up to 20,000 track segments per event
♦ ~1.4 µs total processing time
♦ 90 independent "Track Matching Units" (TMUs)
♦ 1 (large) FPGA chip per TMU
Integration prototype

MCM = PASA+TRAP

DCS board
Trigger & clock distribution, ARM CPU+FPGA, embedded Linux, Ethernet, serial link to the TRAPs …

Detector prototype prepared for the beam test at CERN
MCM tester

Tests automatically the MCM (TRAP+PASA)
- Power supply control
- Check of the reference voltages
- Charge injection to the PASA inputs
- Digitization of the 3 direct PASA outputs
- Sin-wave to the 3 direct ADC inputs
- Stimuli to all digital inputs, readback of all digital outputs

Automatically positioning by video camera and pattern recognition software
Handshaking with the MCM test software
Test of 16 MCMs
(IPE Karlsruhe)
Wafer tester

**Test automatically the TRAP on the wafer:**
- The supply currents
- The serial links and pretrigger
- All internal parts using the CPUs
- The parallel output
- The half of the ADCs using a sin wave generator

![Graph showing ADC output and RES samples vs. samples]

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Conclusions & outlook

- A cheap and compact (4x4cm) mixed mode Multi Chip Module was developed, combining charge sensitive preamplifier/shaper, ADCs, digital filters, processors and readout network

- This makes technically possible the required high integration of the front end electronics in order to readout more than million of channels

- The distributed in space digital computing power enables to process such large amount of data in real time

- In addition the high speed low latency readout network and the Global Tracking Unit provide the possibility to use the detector not only for tracking but also for generating L1 trigger in the system

- The building blocks: PASA & TRAP chips and the MCM are produced/partially produced, the test equipments are developed
TRD Electronics participating institutes

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♦ Institute of Microelectronics, University of Kaiserslautern, Germany
♦ Institute for Physics, University of Heidelberg, Germany
♦ GSI Darmstadt, Germany
♦ University of Applied Sciences Cologne, Communications Engineering, Germany
THANK YOU