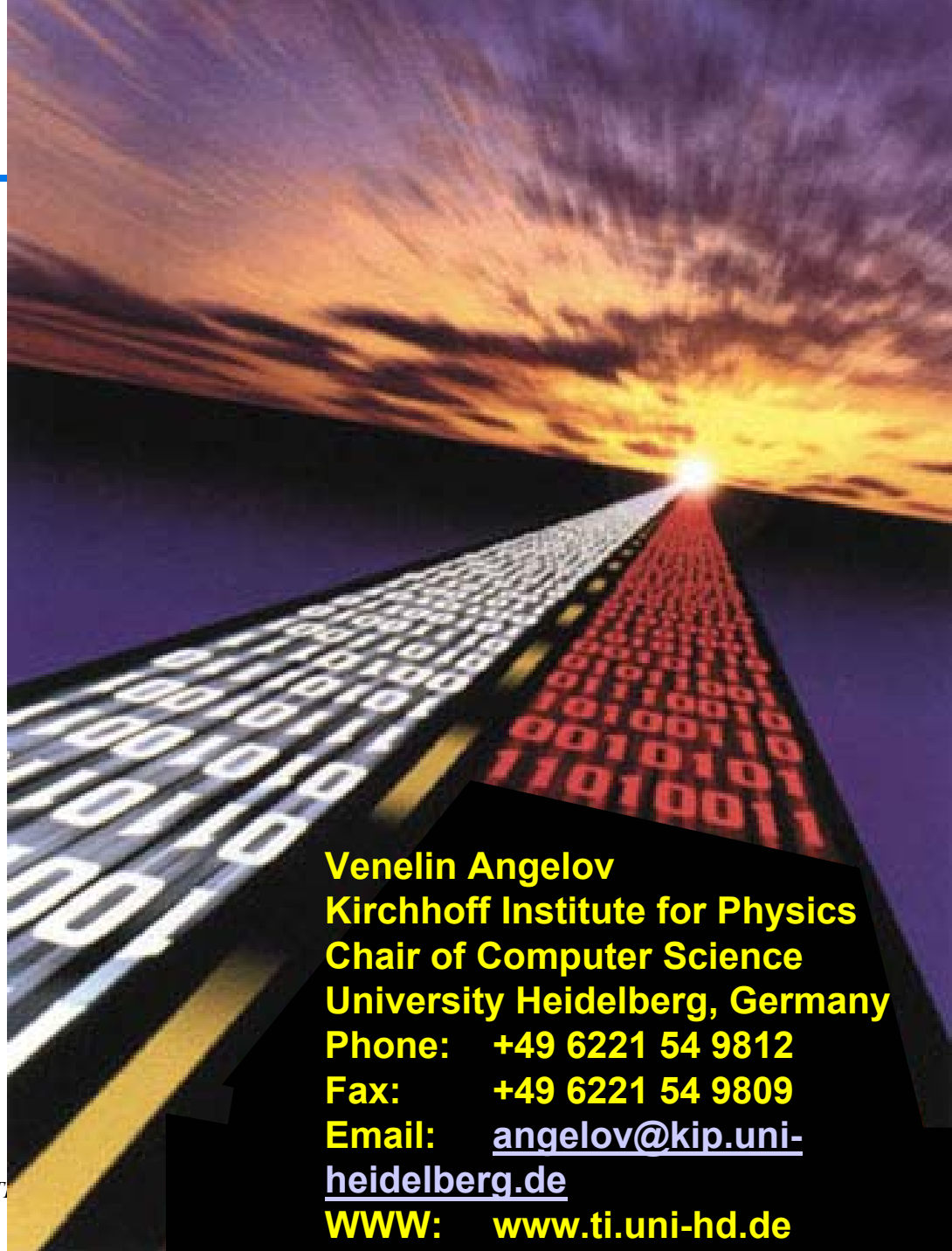
Design and performance of the ALICE TRD frontend electronics

- Introduction
- Multi Chip Module - PASA+TRAP
- Readout tree and GTU
- TRAP and MCM production test
- Conclusions



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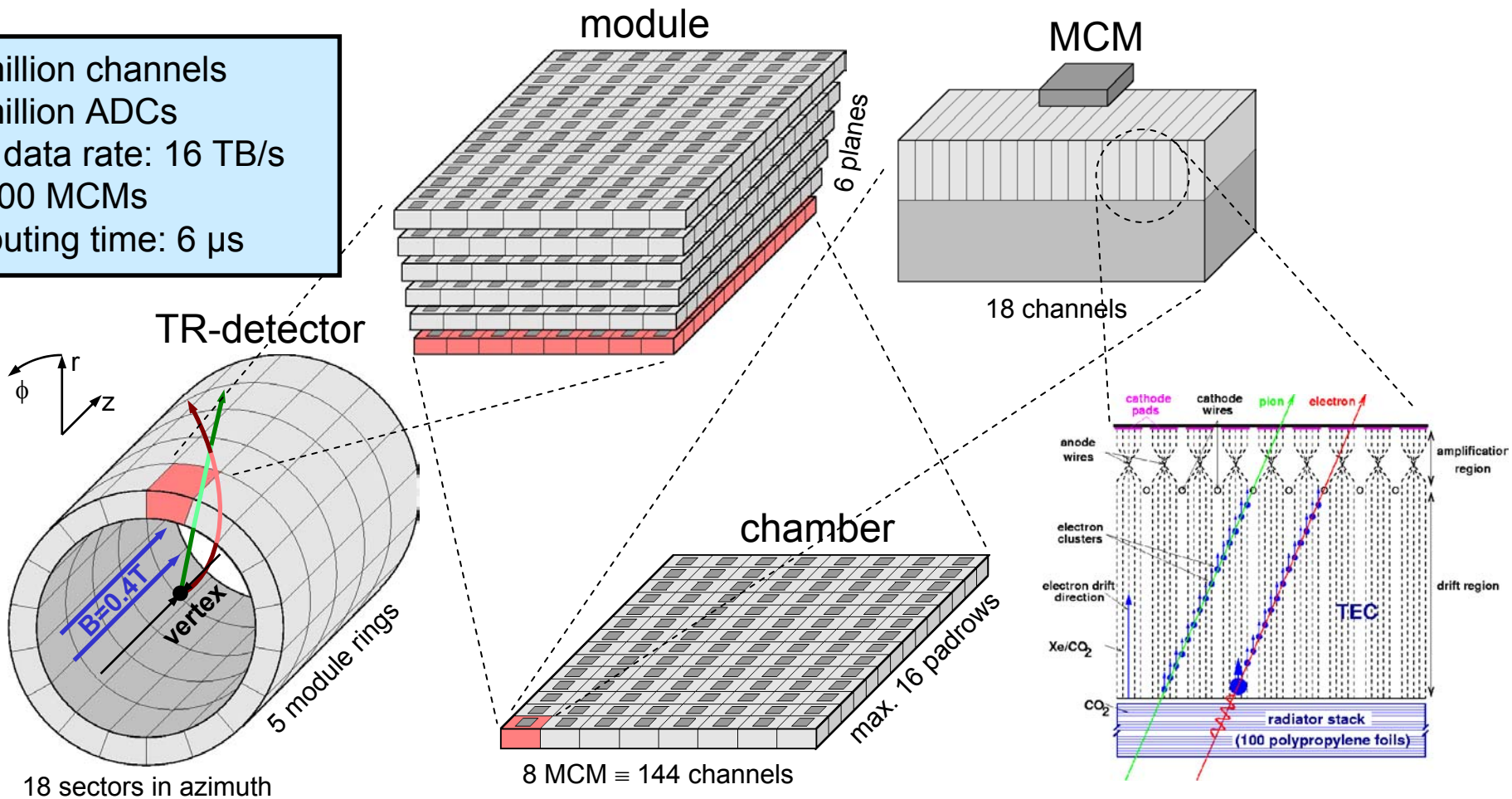
TRD Structure

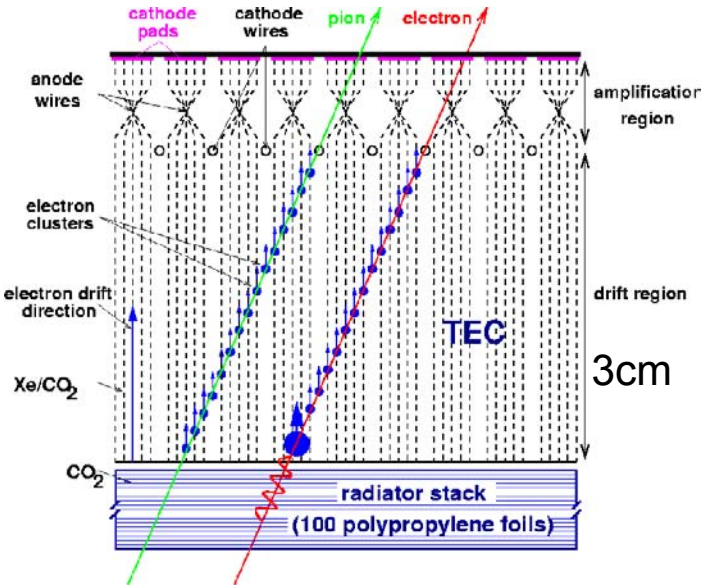
- 1.2 million channels
- 1.4 million ADCs
- peak data rate: 16 TB/s
- ~65000 MCMs
- computing time: 6 μs



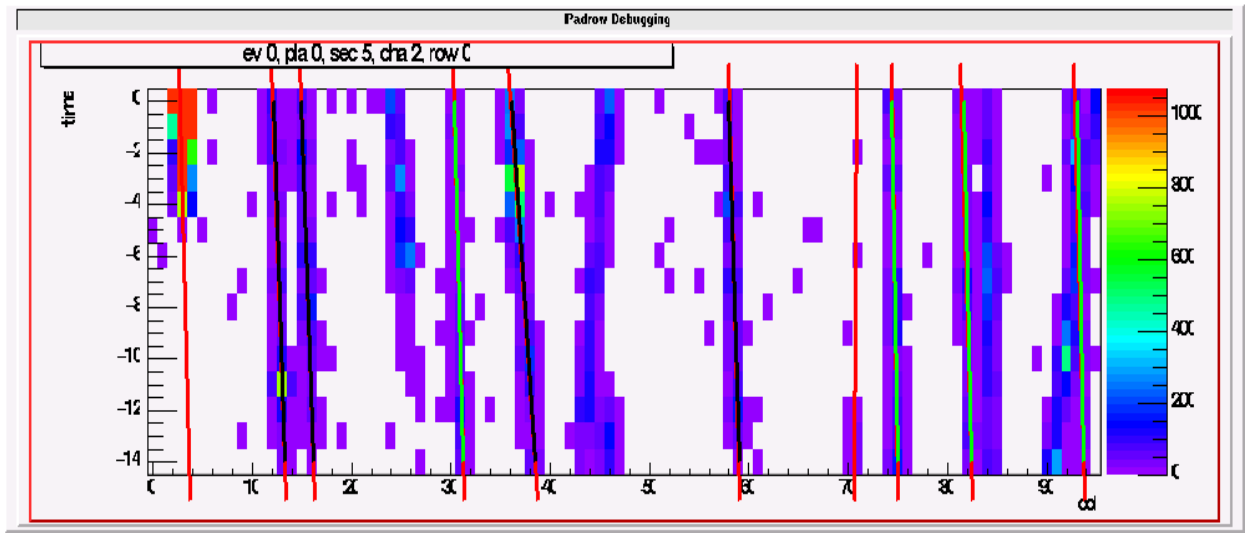
- MCM performs amplification, digitization, straight line fit, readout network

TRD & MCM Functionality

TRD chamber



event display for MCM functionality



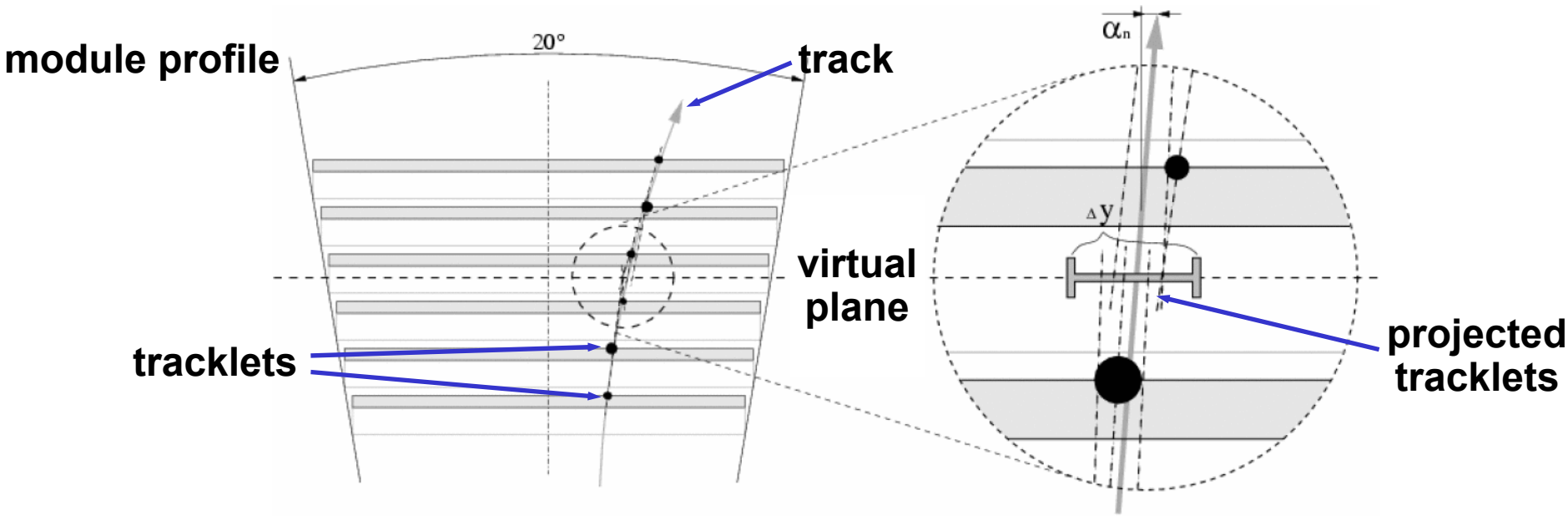
Transition Radiation Detector

- the TRD is a drift chamber to detect the trajectory of charged particles
- in addition a radiator stack in front to cause transition radiation to separate electrons from pions

Multi Chip Module

- the MCM amplifies and digitizes the analog signals and stores the data
- it performs a line fit and ships the track data off the detector to a global tracking unit
- sends zero-suppressed ADC data after L1A

Line Fit & Global Tracking



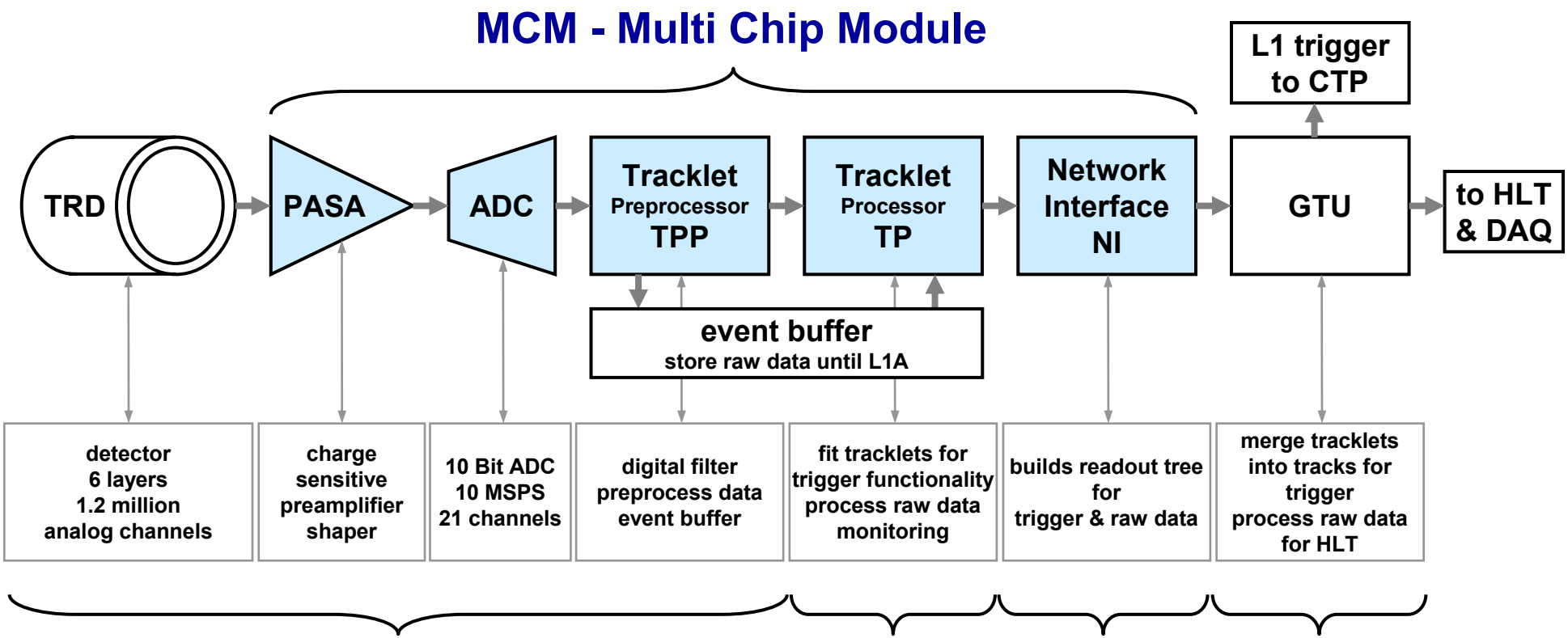
tracklet processor

- straight line fit via a linear regression method
- searching for dedicated patterns (for energy cut and electron - pion separation)
- raw data buffer

global tracking

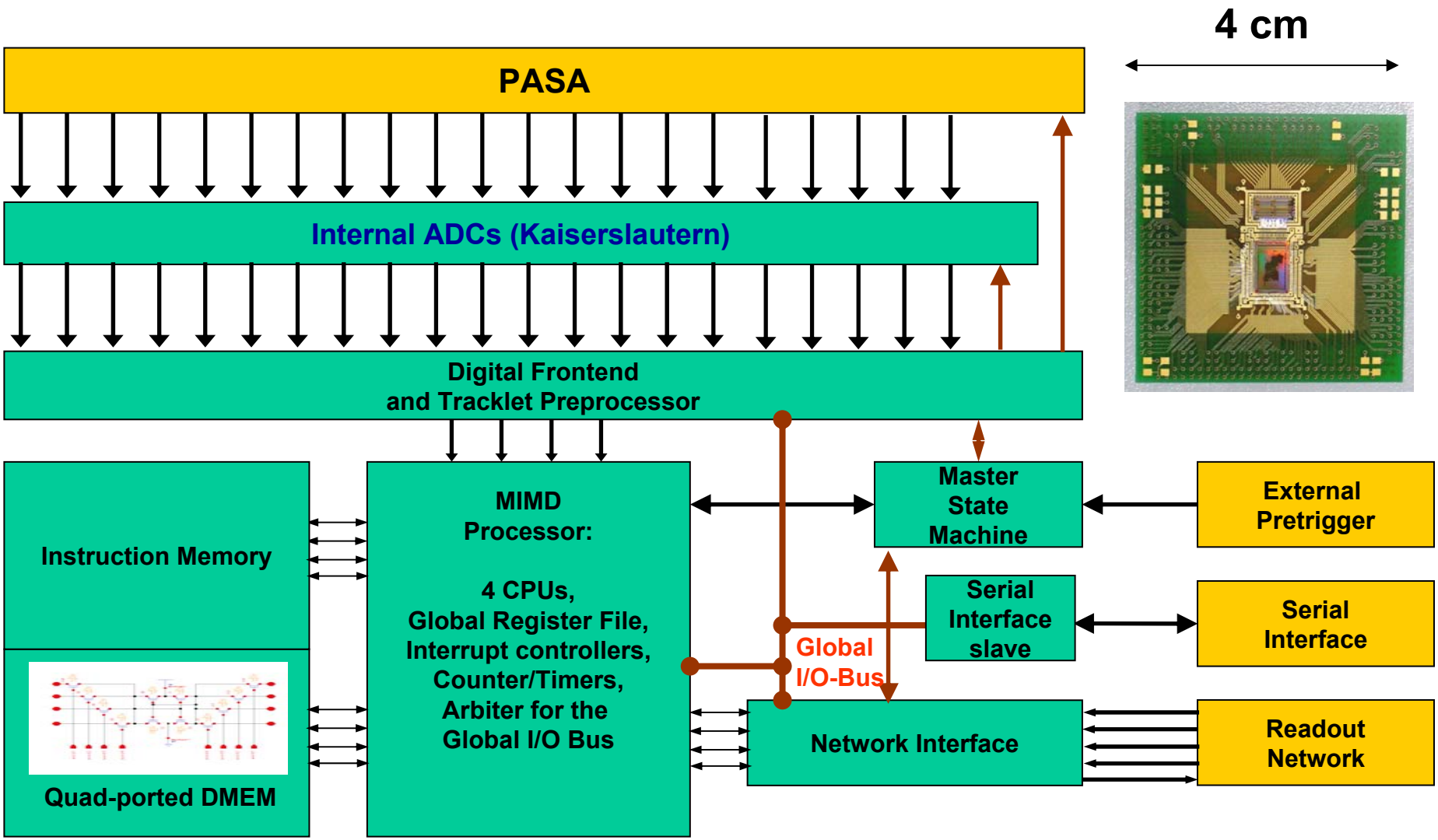
- projection of 'tracklets' to a virtual plane
- searching for tracklets belonging together
- perform cut and generate trigger

Data Flow and Data Reduction

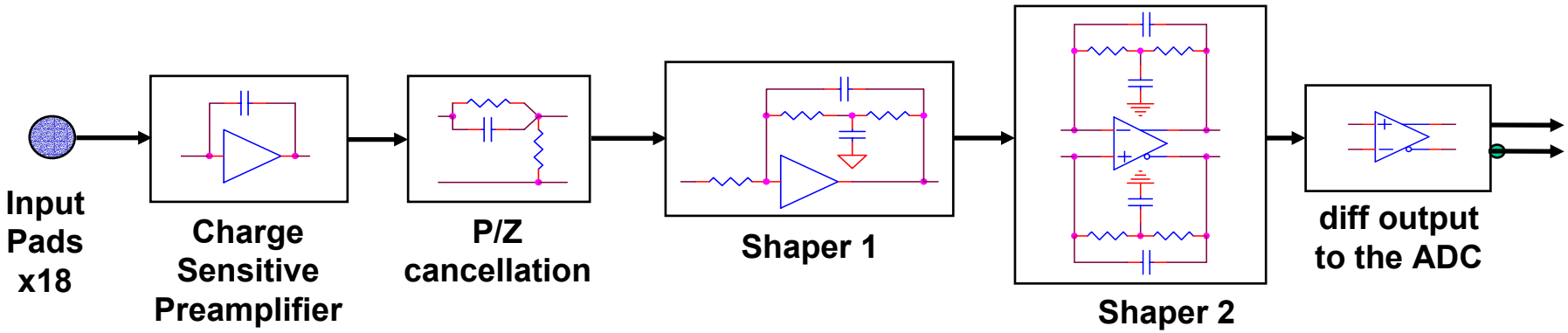


time:	during first 2 µs (drift time)	after 3.5 µs	after 4.1 µs	after 6 µs
data / event:	33 MB		max. 80 KB	some bytes
peak rate:	16 TB/s		600 GB/s	-
mean rate:	257 GB/s		-	-
reduction:	1		~ 400	to trigger decision

Multi Chip Module

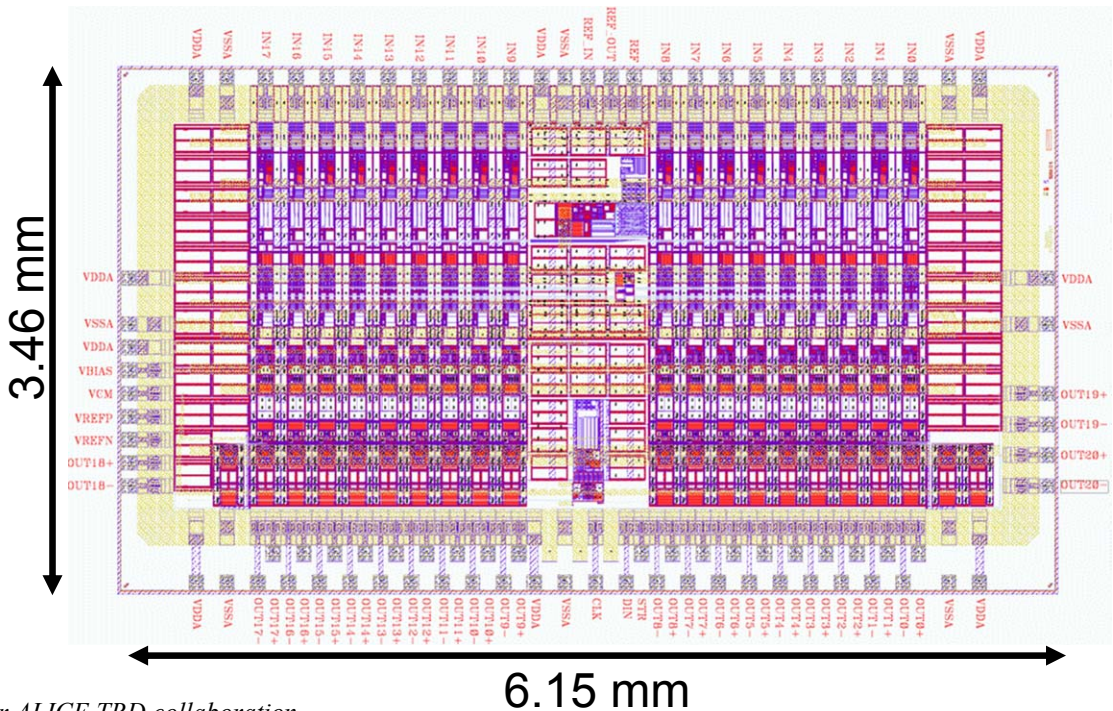


PASA - Preamplifier and Shaper



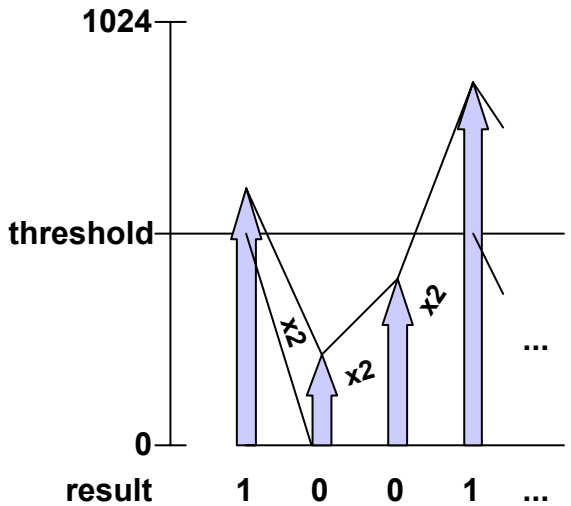
PASA - Preamplifier and Shaping Amplifier

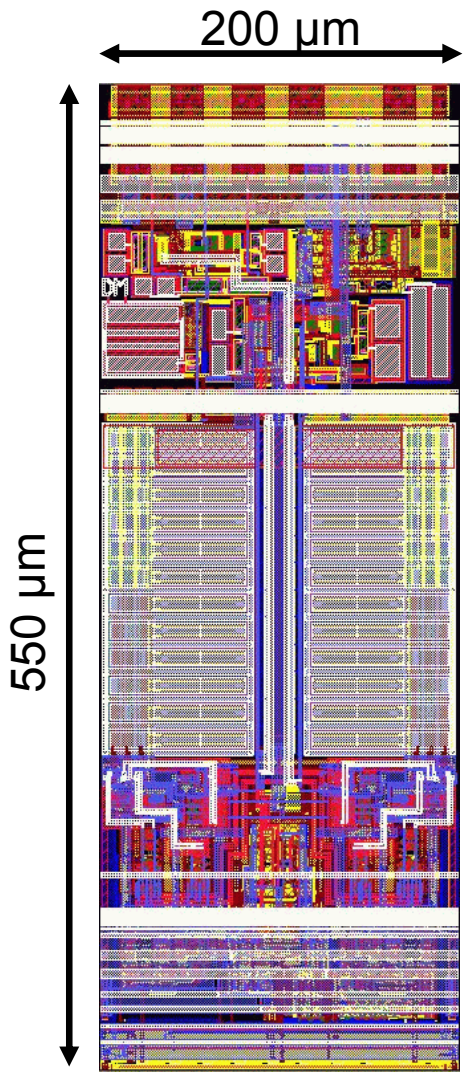
- FWHM: 116 ns
- ENC: 850 electrons at 25 pF
- Gain: 12 mV/fC
- Integral Nonlinearity: 0.3%
- Power: 3.3V, 90 mA / chip
- Process: 0.35µm AMS
- Area: 21.3 mm²
- Yield: 99.8% of the first 20 000 chips



ADC - Analog to Digital Converter

functionality of cyclic ADCs





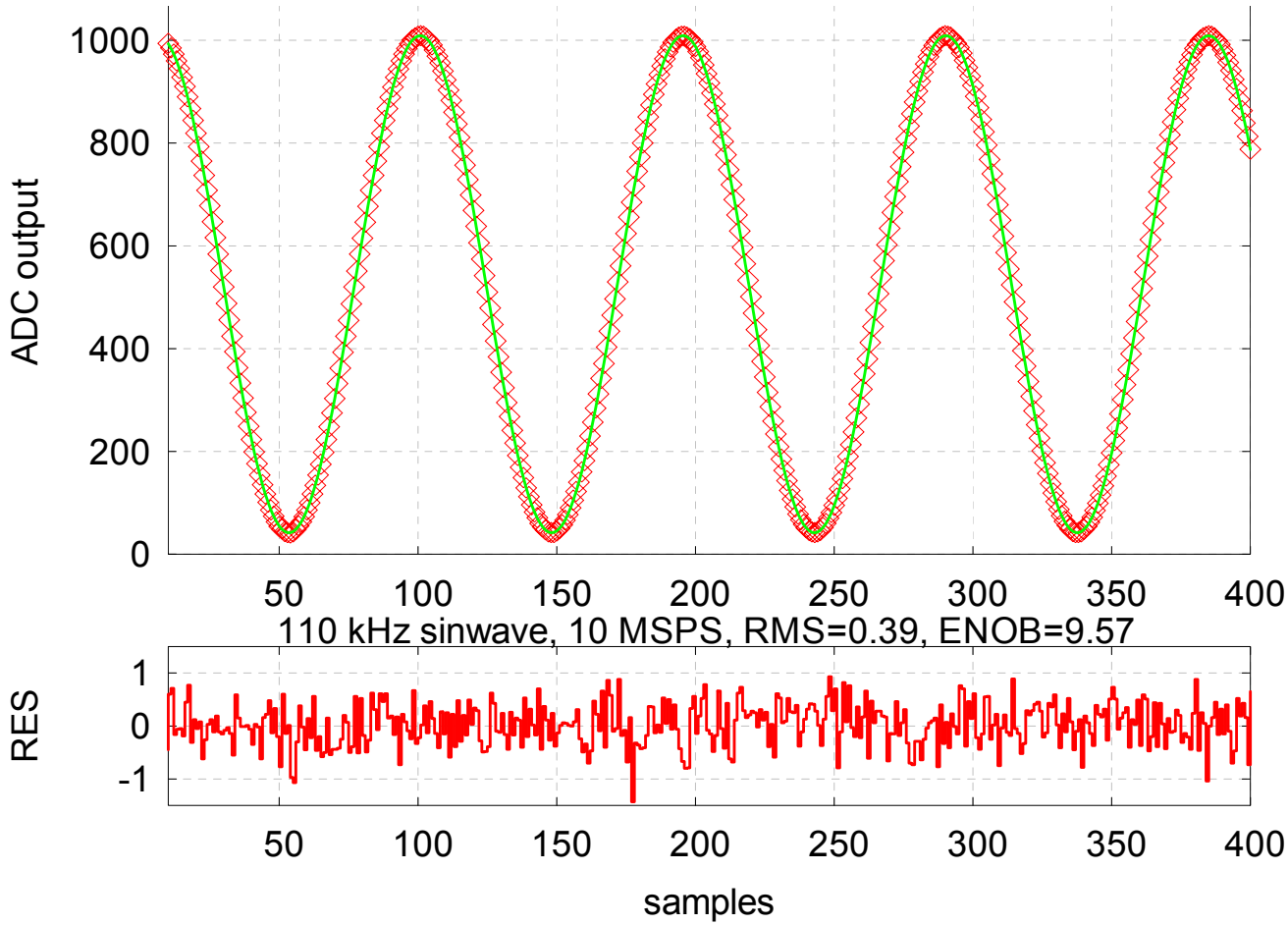
ADC - Analog to Digital Converter
Prof. Tielert, Uni Kaiserslautern

- 10 Bit, 10 MSPS, no latency
- Cyclic ADC, 240 MHz internal
- ENOB: 9.5
- Power: 10 mW / channel (programmable)
- Area: 0.11 mm² (550 x 200 µm²)

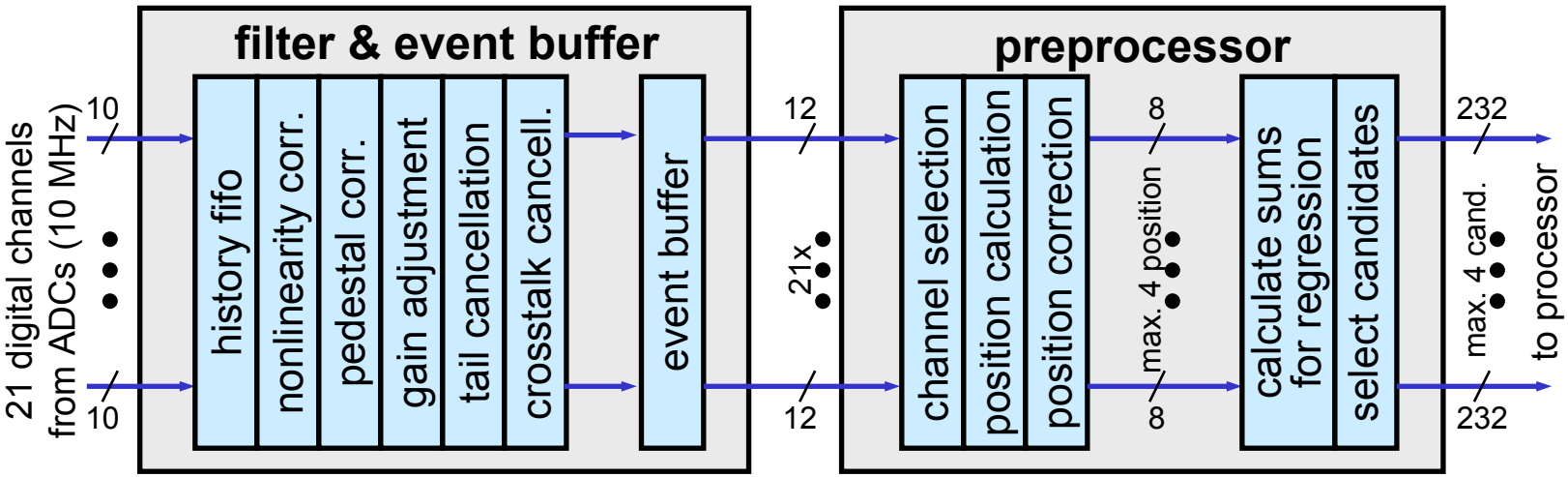
ADC Performance

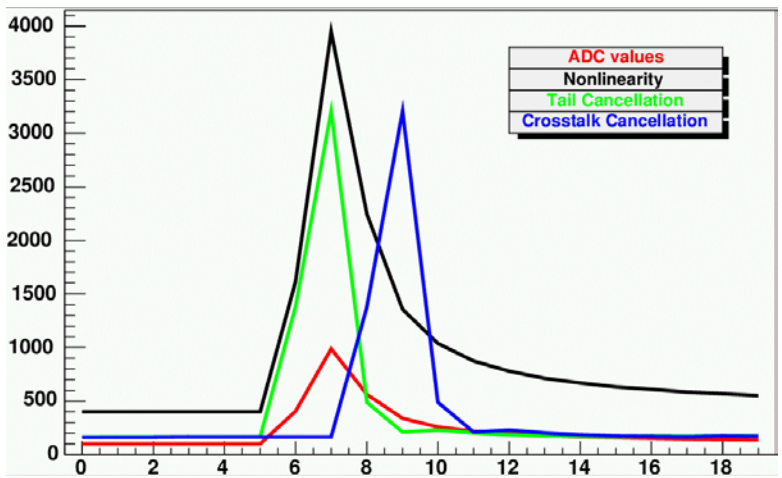
Sinwave measured using one CPU to copy the ADC data into the memory.

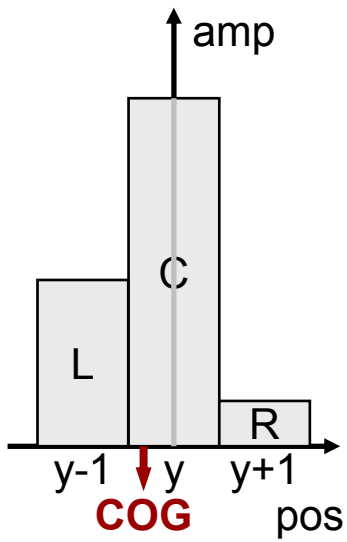
Note that by the normal operation in the detector the ADC data will be processed and stored without turning on the CPUs.

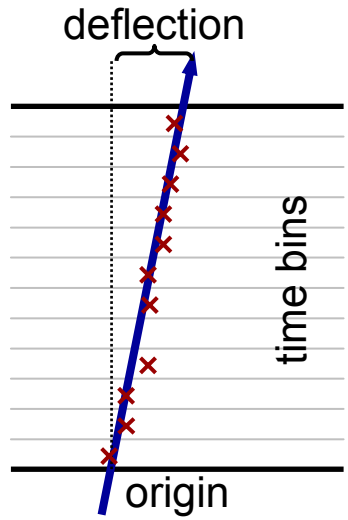


Filter & Preprocessor









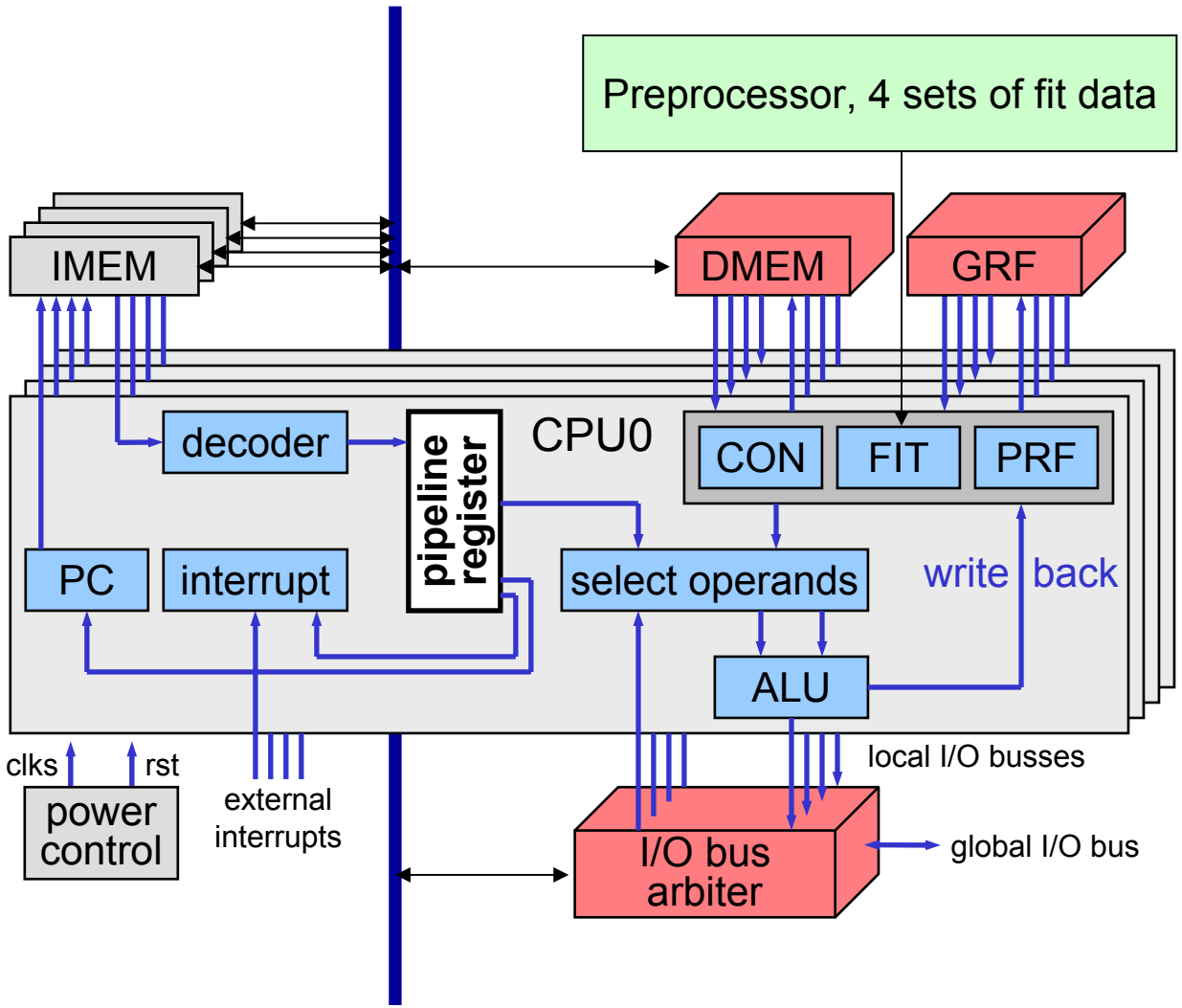
MIMD Processor

MIMD processor

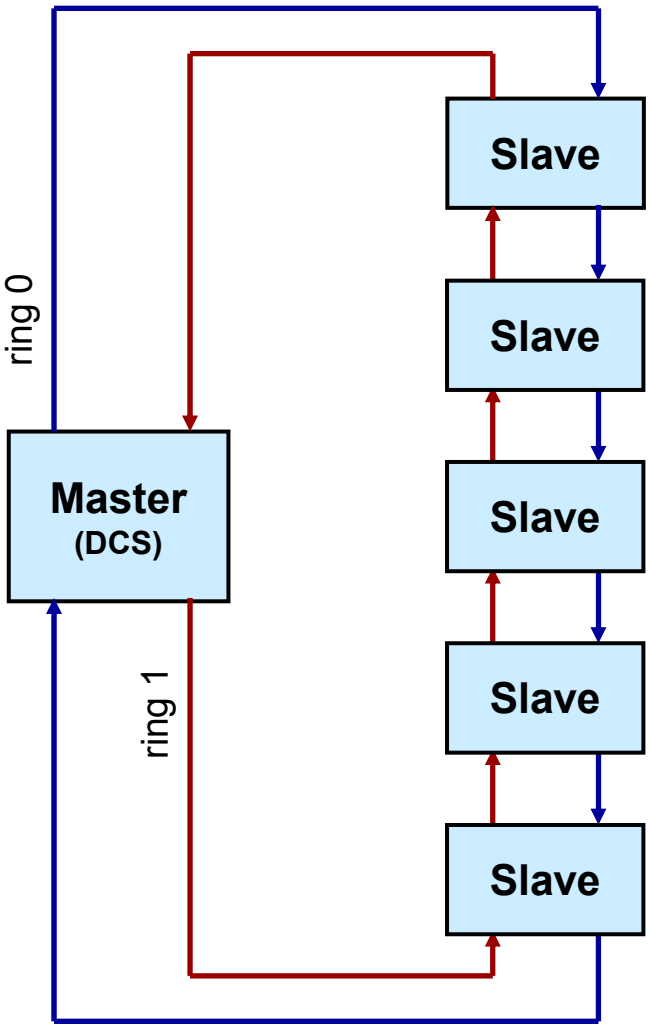
- 4 CPUs
- shared memory / register file
- global I/O bus arbiter
- separate instruction memory
- coupled data & control paths

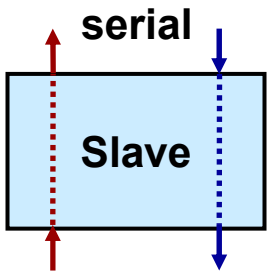
CPU

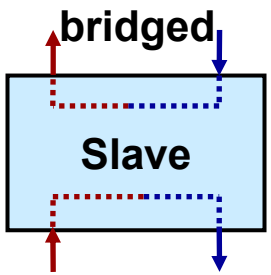
- Harvard style architecture
- two stage pipeline
- 32 Bit data path
- register to register operations
- fast ALU
  - 32x32 multiplication
  - 64/32 radix-4 divider
- maskable interrupts
- synchronization mechanisms



SCSN - Slow Control Serial Network

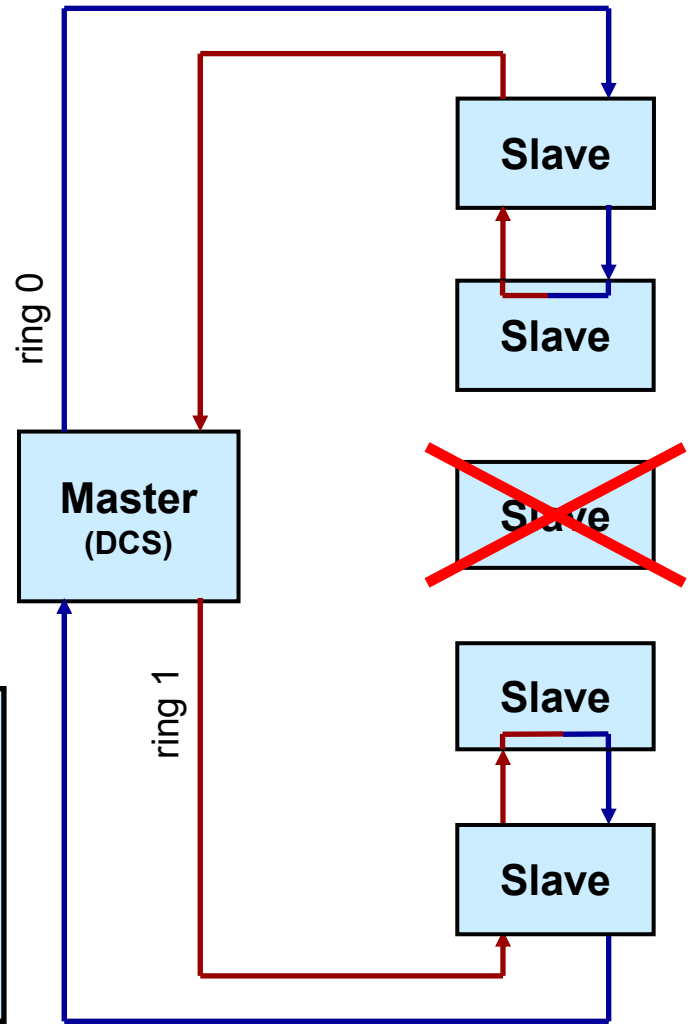




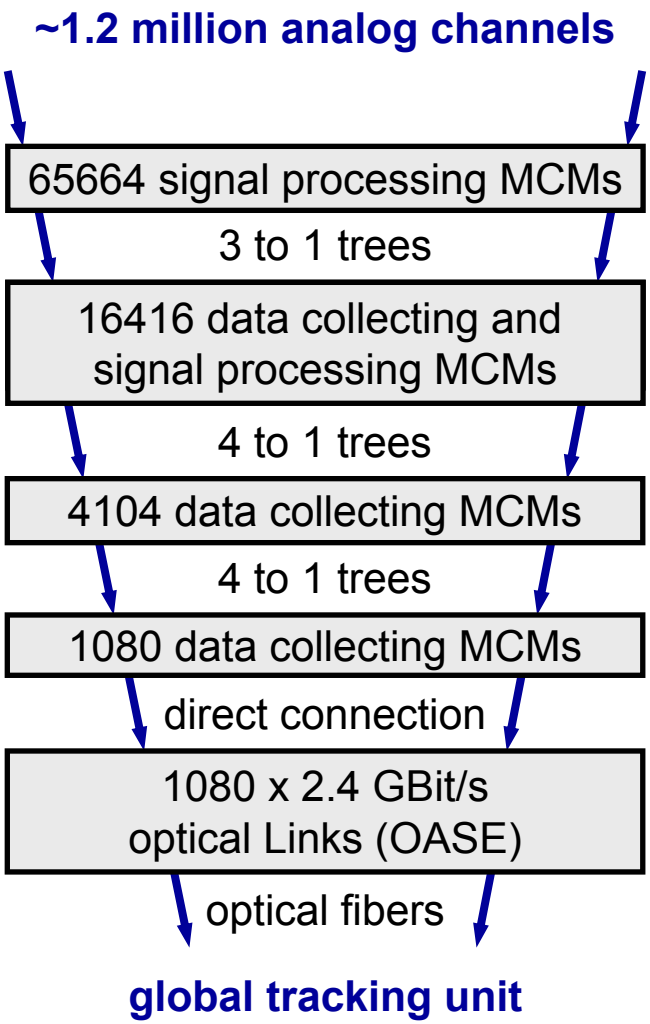


SCSN

- Up to 126 slaves per ring
- CRC protected
- 24 MBit/s transfer rate
- 16 addr., 32 data-bits/frame



Readout Tree



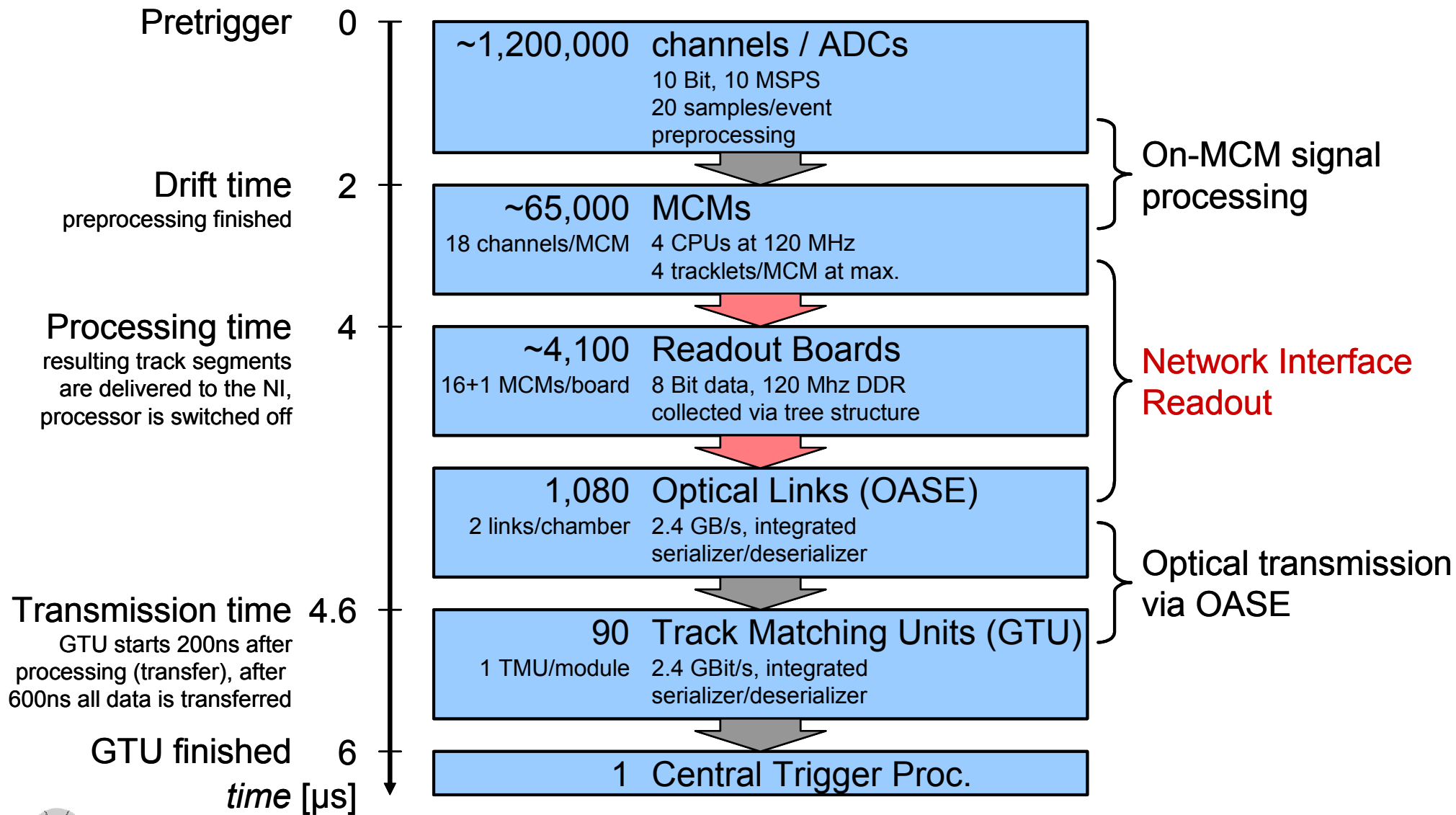
NI - Network Interface

- I/O interfaces
  - direct access via local I/O interfaces
  - global I/O configuration and status registers
- 4 input, 1 output ports
  - 8 Bit data at 120 MHz DDR (240 MB/s)
  - + strobe, parity and spare bit
- data resynchronization
- input fifos (256 Bytes / port)
- 1 clock cycle input to output latency incl. data resynchronization

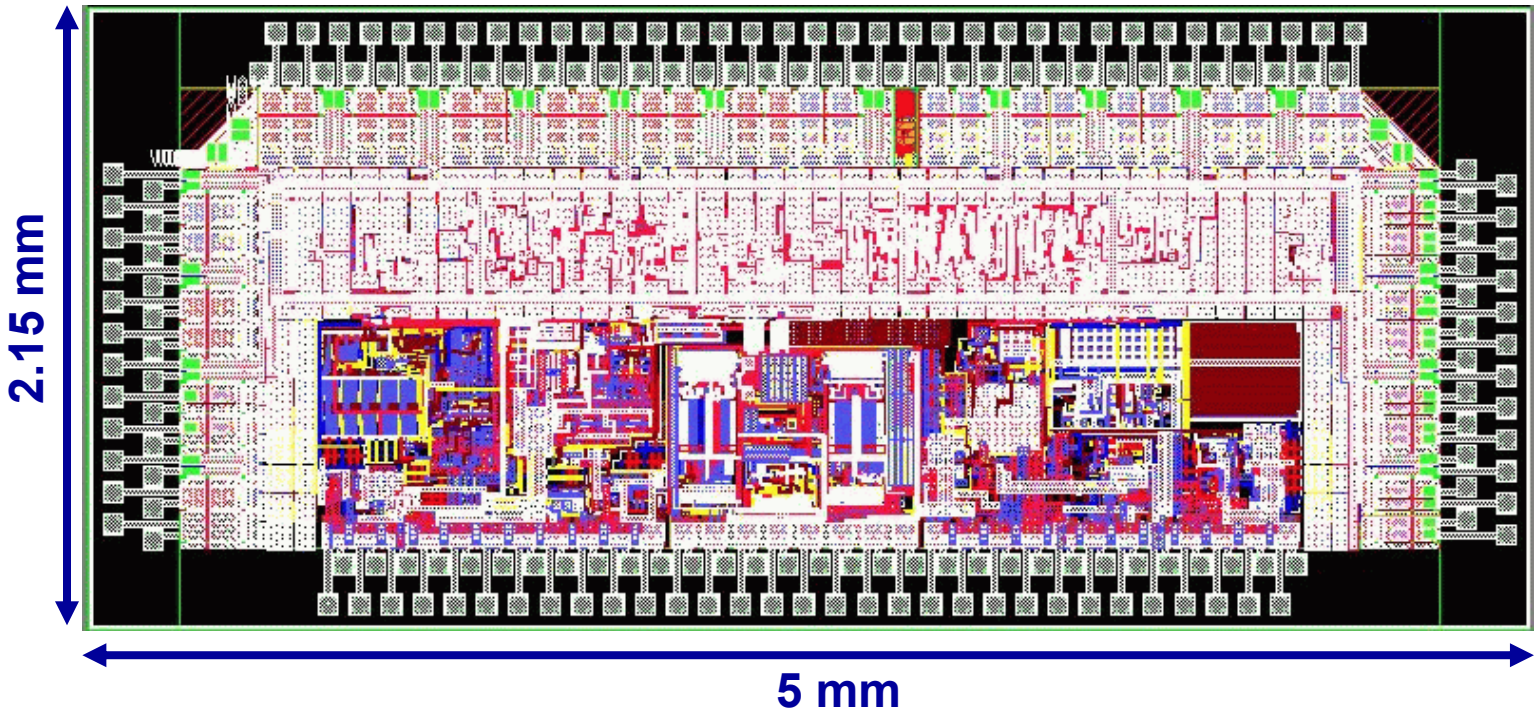
Readout

- collecting data of 65664 MCMs
- interface to the GTU are 1080 optical links with 2.4 GBit/s each
- readout latency: ~200 ns
- full trigger readout within 600 ns

Detector Readout



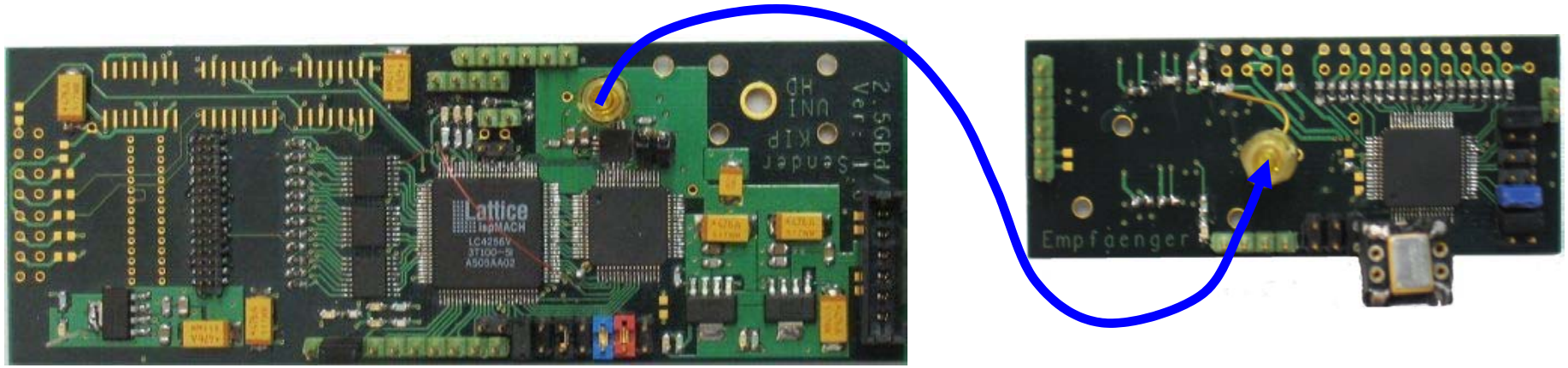
OASE



OASE - Optical Advanced SErializer
Prof. Brüning, Uni Mannheim
Prof. Tielert, Uni Kaiserslautern

- 8 Bit at 120 MHz DDR parallel ⟷ 2.4 GBit/s serial tranceiver
- SCSN and I²C configuration interfaces, JTAG
- pins to directly connect laser diodes for on-chip connection

OASE backup solution



Replacement for the OASE board with the same connector and speed

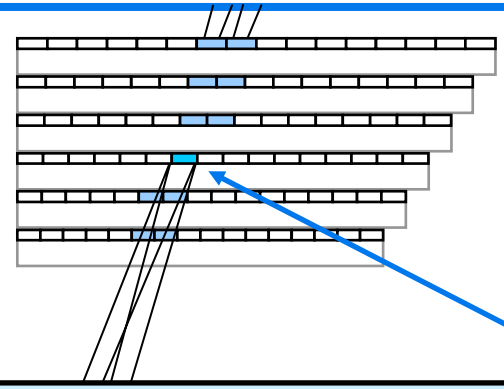
- 8 Bit at 120 MHz DDR parallel to 16 bit SDR 120 MHz conversion using CPLD
- Commercial gigabit serializer from Texas Instruments
- Driver for the laser diode

Receiver board for testing of the gigabit serializer board

- Amplifier for the photodiode
- Commercial gigabit deserializer from Texas Instruments

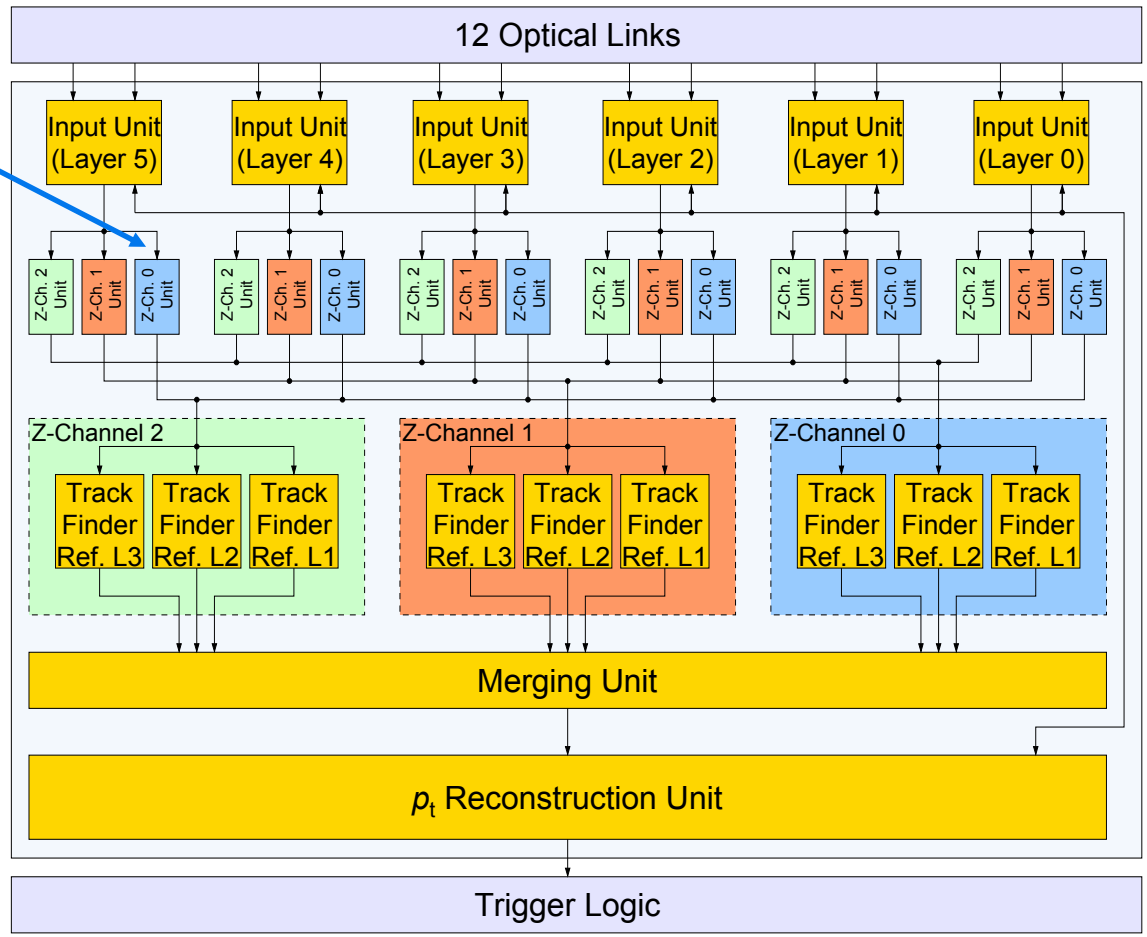
The main drawback of this solution is the higher price and the larger number of components

GTU Implementation



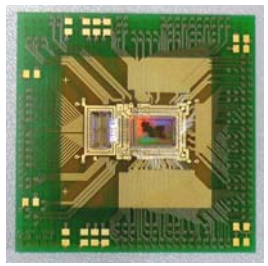
Global Tracking Unit

- receive data from 1080 optical links
- process up to 20,000 track segments per event
- ~1.4 µs total processing time
- 90 independent "Track Matching Units" (TMUs)
- 1 (large) FPGA chip per TMU



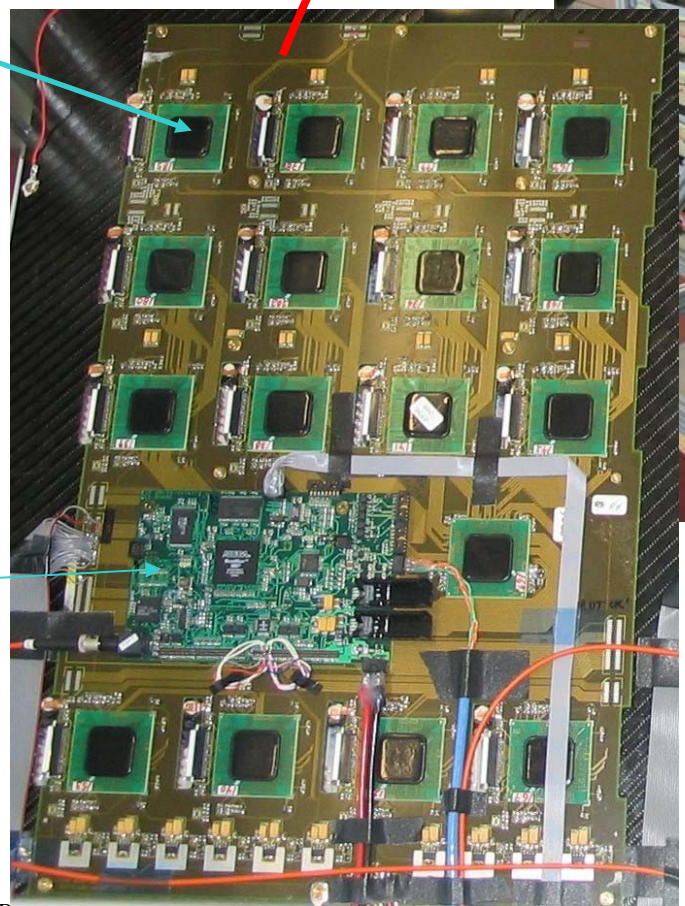
Integration prototype

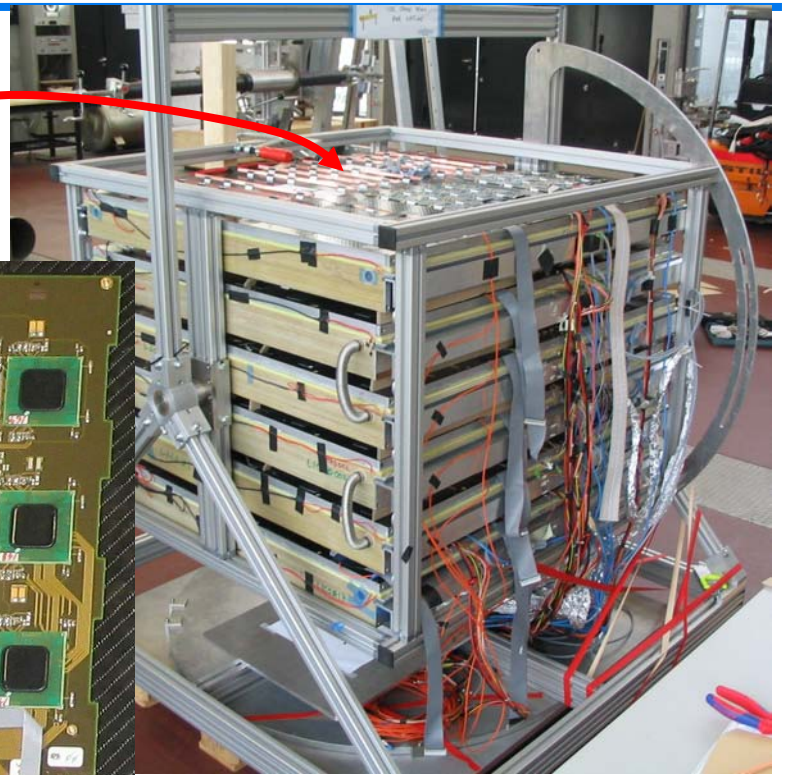
MCM = PASA+TRAP



DCS board

Trigger & clock distribution, ARM CPU+FPGA, embedded Linux, Ethernet, serial link to the TRAPs …

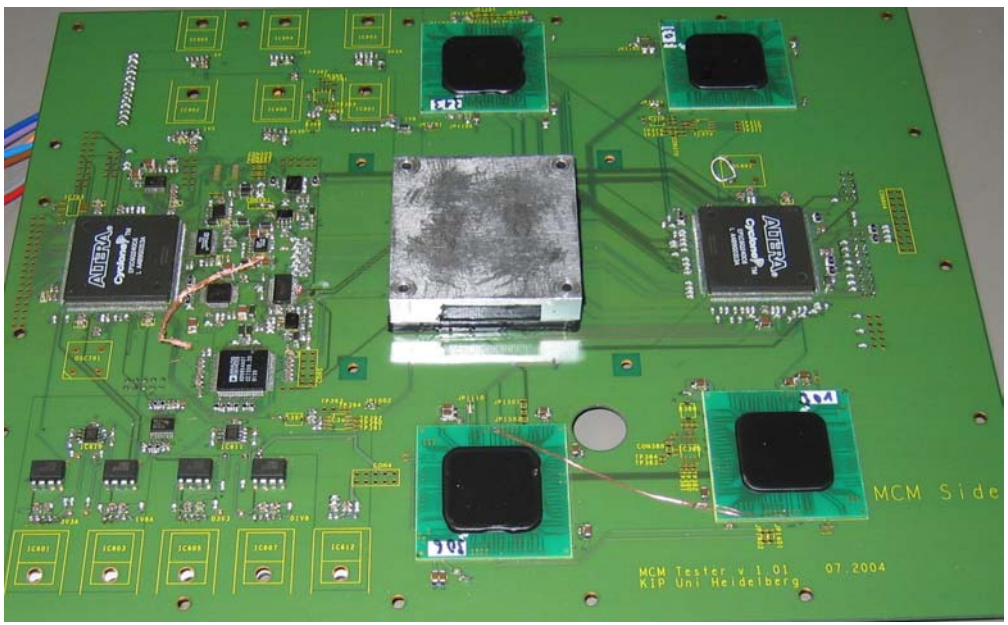




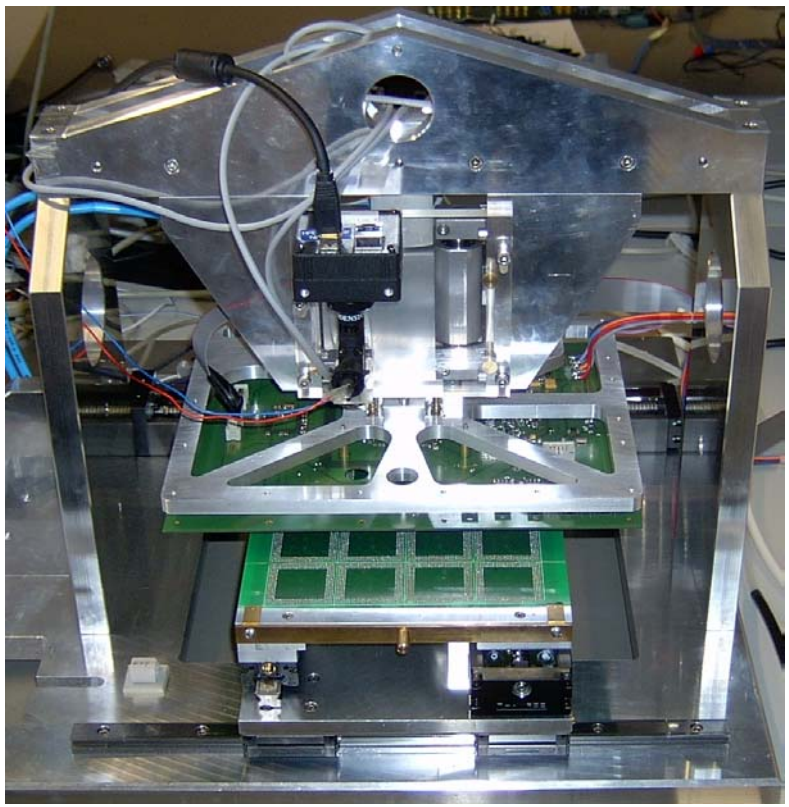
Detector prototype prepared for the beam test at CERN

MCM tester

Tests automatically the MCM (TRAP+PASA)
- Power supply control
- Check of the reference voltages
- Charge injection to the PASA inputs
- Digitization of the 3 direct PASA outputs
- Sin-wave to the 3 direct ADC inputs
- Stimuli to all digital inputs, readback of all digital outputs



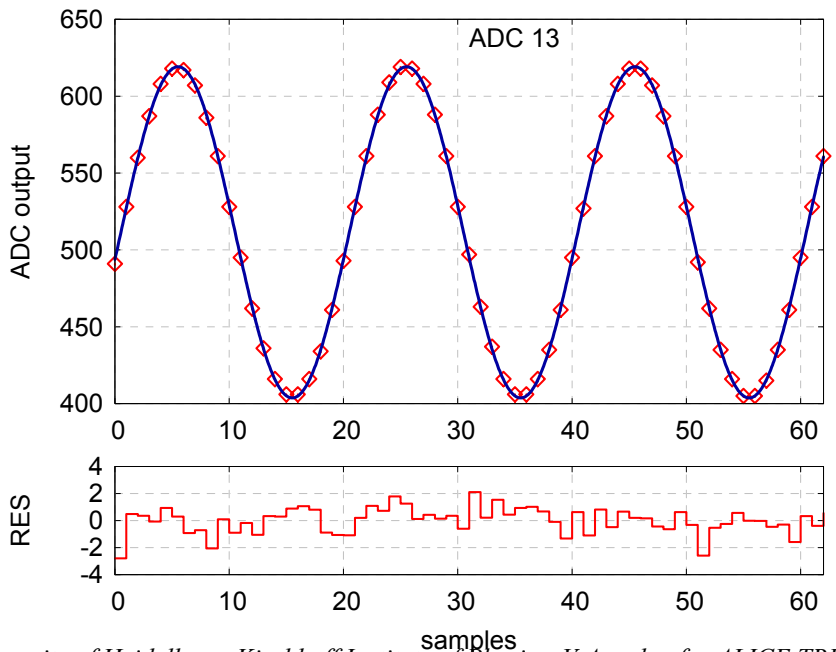
Automatically positioning by video camera and pattern recognition software
Handshaking with the MCM test software
Test of 16 MCMs
(IPE Karlsruhe)

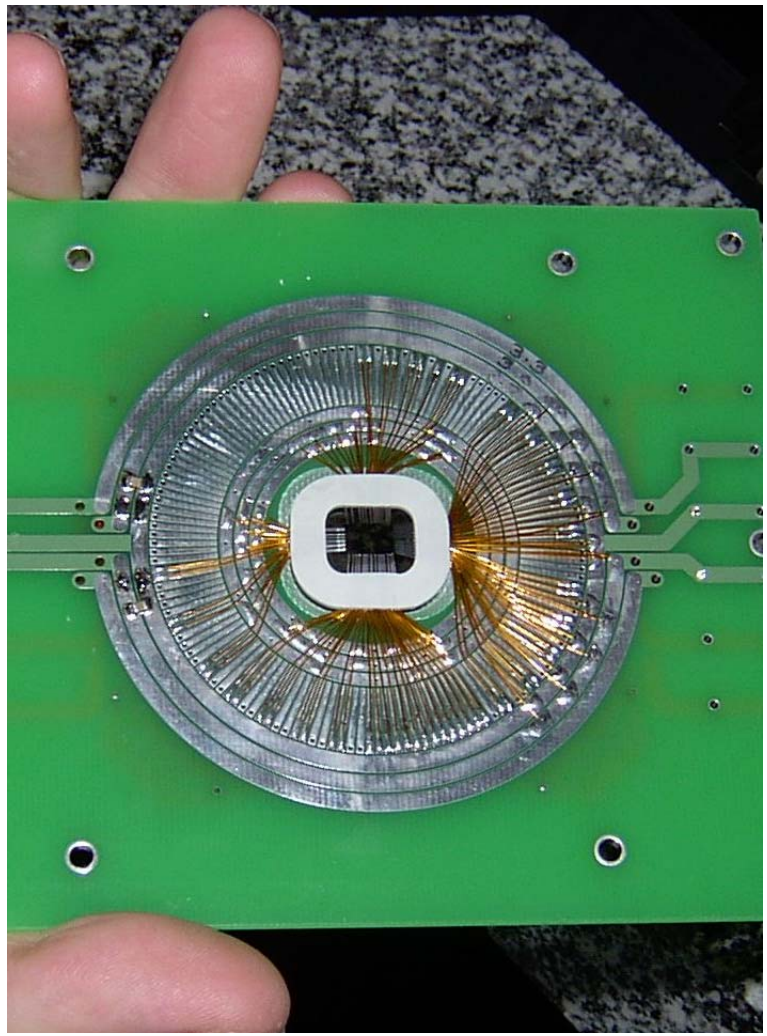


Wafer tester

Test automatically the TRAP on the wafer:

- **The supply currents**
- **The serial links and pretrigger**
- **All internal parts using the CPUs**
- **The parallel output**
- **The half of the ADCs using a sin wave generator**





Conclusions & outlook

- A cheap and compact (4x4cm) mixed mode Multi Chip Module was developed, combining charge sensitive preamplifier/shaper, ADCs, digital filters, processors and readout network
- This makes technically possible the required high integration of the front end electronics in order to readout more than million of channels
- The distributed in space digital computing power enables to process such large amount of data in real time
- In addition the high speed low latency readout network and the Global Tracking Unit provide the possibility to use the detector not only for tracking but also for generating L1 trigger in the system
- The building blocks: PASA & TRAP chips and the MCM are produced/partially produced, the test equipments are developed

TRD Electronics participating institutes

- Kirchhoff Institute for Physics, University of Heidelberg, Germany
- Institute of Microelectronics, University of Kaiserslautern, Germany
- Institute for Physics, University of Heidelberg, Germany
- GSI Darmstadt, Germany
- University of Applied Sciences Cologne, Communications Engineering, Germany

THANK YOU