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Design and performance of the ALICE TRD front-end electronics

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Abstract

The Transition Radiation Detector (TRD) of the ALICE experiment at CERN incorporates 1.2 million channels which are individually read out and processed. The front-end electronics (FEE) utilizes two custom chips: an 18 channel analog preamplifier and shaper (PASA) and a mixed-signal chip, performing 10 bit analog-to-digital conversion, event buffering and local tracking (TRAP). Both chips together are packaged as a $4 \times 4\,cm^2$ ball grid array multi chip module (MCM). More than 65 k of these will be integrated on the detector. In fall 2004, a small prototype implementing 140 MCMs was successfully tested at CERN. The MCMs demonstrate an ADC performance of 9.5 effective bits while the digital back-end is operating, including four RISC processors. The electronic noise of the PASA mounted on the detector was measured with the digital back-end to be below 1200 electrons.

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1. Introduction

The Transition Radiation Detector (TRD) of the ALICE experiment has the primary function to identify high p_t electrons and to deliver fast trigger information [1–3] within a few microseconds after the interaction. The number of analog channels to be processed is enormous—over 1.2 million, which is sampled at 10 MHz with 10 bits, leading to a total amount of raw data in one event of more than 33 Mbytes, spatially distributed over a barrel with a mean diameter of 6.6 m, length of 7 m and a total active area of all layers of $736\,m^2$. This implies a very high required integration density of the front-end electronics [4] and emphasizes the requirements on the total power dissipated by all electronic components.

The tracks of the charged particles are reconstructed using the time-dependent current induced on the detector cathode pads. The position of the charge clusters can be determined from the charge sharing between neighbouring pads. The other coordinates are hit padrow and the time, which can be translated into distance to the padplane.

The most suitable basic building block for this detector is a Multi Chip Module (MCM), consisting of one pure analog chip, the Preamplifier and Shaping Amplifier (PASA) [5] and one mixed mode TRAcklet Processor (TRAP) [6,7] chip. The MCMs are hosted by Readout Boards (ROB) [8]. They integrate power supply, Detector Control System (DCS) interface boards and Gigabit optical links.

In fall 2004, a prototype of the detector consisting of six layers and FEE was successfully tested at CERN. This prototype is still operating and actively used to optimize the noise performance.

2. Multi Chip Module

The MCM is the basic front-end electronics building block, consisting of two chips. It has 18 charge sensitive inputs, three differential PASA outputs, three differential ADC inputs and several digital ports, see Fig. 1.

2.1. PASA

The PASA chip amplifies and shapes the analog signals from 18 detector pads.

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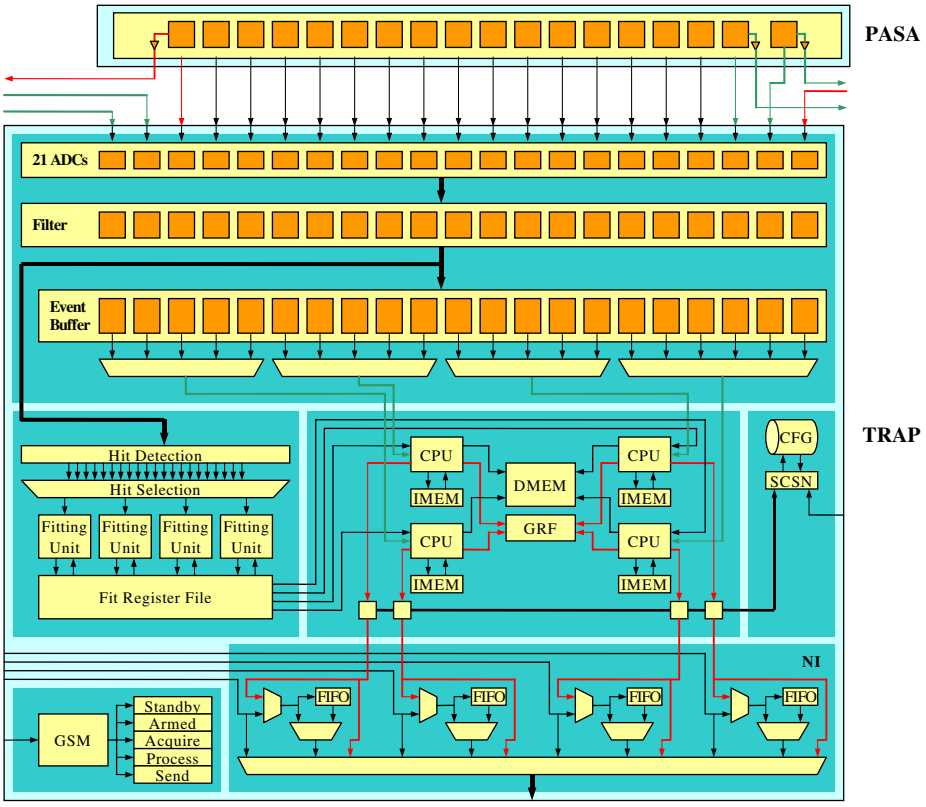

Fig. 1. The MCM building blocks.

The main part of the PASA consists of a preamplifier, a pole-zero network, one single-ended second-order bridged-T filter, one fully differential second-order bridged-T filter, a wide swing common-mode feedback amplifier, two noninverting stages, a self-adaptive bias network, three internal references, and a threshold reference self-biasing circuit with a startup circuit is also included. This chip was developed in 0.35 μm AMS technology. The gain is about 12 mV/fC, the pulse width is 116 ns (FWHM), equivalent noise charge 850 e at 25 pF and power consumption about 15 mW/channel. The outputs are differential, with a maximum amplitude of 2 V peak-to-peak. Three of the boundary channels have additional outputs, which are fed to the neighbouring MCMs. This is necessary in order to correctly process tracks situated at the boundary of two MCMs.

2.2. TRAP

The TRAP chip performs analog-to-digital conversion, digital filtering and preprocessing, calculation of the track parameters, data formatting and shipping over a fast network. The ADCs provide 10 bit samples at a rate of 10 MHz. Their size per channel is 0.11 mm^2 and the power consumption is typically 12.5 mW/channel [9]. They operate internally at 240 MHz and have a very low conversion latency of about 1.5 samples. Their effective number of bits is typically about 9.5, measured using the CPUs. The input full range is programmable from 2 to 2.8 V.

The digital processing is done in two steps. First, during the drift time, the ADC data pass through digital filters and correction stages like: non-linearity, gain, pedestal, tail cancellation, crosstalk corrections. Either the raw ADC data or the output of the enabled filters are stored in the event buffers. The hit-detection units recognize valid charge clusters. Up to four of the largest clusters are selected and further processed. More than four tracks inside the associated geographic range of single MCM are very unlikely. The position of the charge cluster is calculated on the basis of the charge sharing using the ADC data from three neighbouring pads. The deviation of the position from the centre of gravity is tabulated and used to perform a precise coordinate calculation. In order to perform a straight line fit one needs to accumulate some well-known sums. This is done as the last step in the preprocessor inside the TRAP chip.

After the end of the drift time, the four RISC CPUs running at 120 MHz [10] are started to continue the fitting process. The accumulated sums are mapped as CPU read-only registers. If necessary the fit parameters of two adjacent channels are merged together. The CPUs check whether the track fulfils some programmable constrains for slope, fit quality and estimated electron/pion probability. At the end of the processing the CPUs format the output results as one 32 bit word per tracklet and send it via the

readout tree [11]. It operates at 120 MHz with double data rate and effective bandwidth of 240 MBytes/s.

The maximum electron drift time in the TRD gas and thus the maximum signal length is about 2 μs, the CPU processing and data shipping time is about 1 μs. To optimize the parallel processing of the CPUs, a full custom quad-ported memory has been integrated into the TRAP design.

In order to improve the stability of the digital part in radiation environment, all state machines, instruction and data memory blocks are hamming protected. Single bit flips are corrected automatically, double bit flips are detected and counted. In order to test the MCM independently in situ, two features have been added. The PASA chip implements a programmable test pattern generator, allowing the TRAP chip to program a charge amount to be injected into the PASA input at a list of channels, selected by a programmable channel mask. Second, the event buffer in the TRAP chip can be preloaded with test events and used as a defined data source instead of the ADCs.

3. Additional building blocks

As the front-end electronics becomes more and more flexible and intelligent, it needs complex initialization after turning on the power and a special procedure to optimize all parameters. The TRAP chip has a redundant, dedicated serial interface for the configuration and simple tests. The TRAPs on the detector are connected in groups of about 35 chips on two ROBs in daisy-chained networks, the slow control serial networks (SCSN). A highly universal and compact board (DCS) was developed, incorporating an FPGA with an embedded processor capable of running Linux operating system, using ethernet as network interface. It serves as SCSN master and is responsible for the configuration of the TRAP chips on six or eight ROBs and for controlling the power supplies.

The fast transfer of the tracklets and raw data off the detector is done using 1080 optical serial links operating at 2.5 Gb/s. Each link sends the data from up to 64 MCMs on four ROBs to the Global Tracking Unit (GTU). The GTU consists of 90 modules with 12 optical receivers, a large FPGA and memory. A fast algorithm implemented in the FPGA performs a search for complete tracks in the data from all six layers of the detector.

A fully automated module was designed for the test of the TRAP chip on the wafer and of the MCMs.

4. Test results

The production of the PASA chips has been completed, and a significant part of them has already been tested on the wafers. The production of the TRAP chips and of the MCMs has been started.

In fall 2004, a detector prototype set-up has been assembled. It is a stack of six detector layers, incorporating 139 MCMs on eight ROBs. It has been used for data acquisition of about 60 GB within a beam-time at the Proton Synchrotron (CERN, Geneva). In addition a test of the signal processing capabilities has been done. The digital filter behave like expected. A comparison of the online computed track parameters with offline analysis shows a quite good agreement. Only minor differences are caused by internal truncations in the TRAP arithmetics in contrast to the floating point operations of the offline analysis. After the CERN beamtime, the prototype stack is used for on-going optimizations of runtime conditions, filter and tracking parameters. Therefore, cosmic radiation is used as a signal source. Fig. 2 shows an event in four layers of the detector prototype. The data of each layer are acquired by a set of four neighbouring MCMs.

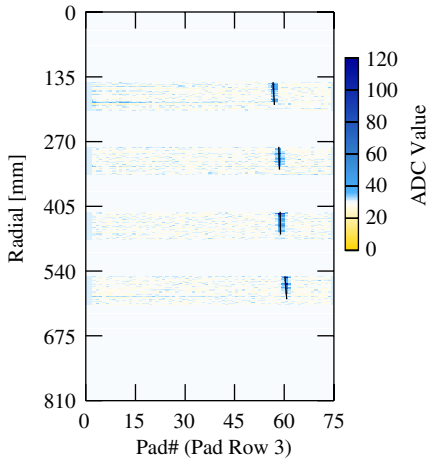

Fig. 2. Example event with a track crossing four layers, the ADC values are colour mapped.

5. Conclusions

The FEE for the ALICE TRD has reached the final level and is ready to be integrated into the actual detector. It incorporates outstanding online processing capabilities like hardware filtering, particle tracking and data transmission. Its design is optimized for low power, low noise and high flexibility. Tests in a prototype set-up have shown stable operation with about 2500 analog channels. The production of the chips, MCMs and ROBs has been started recently.

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