

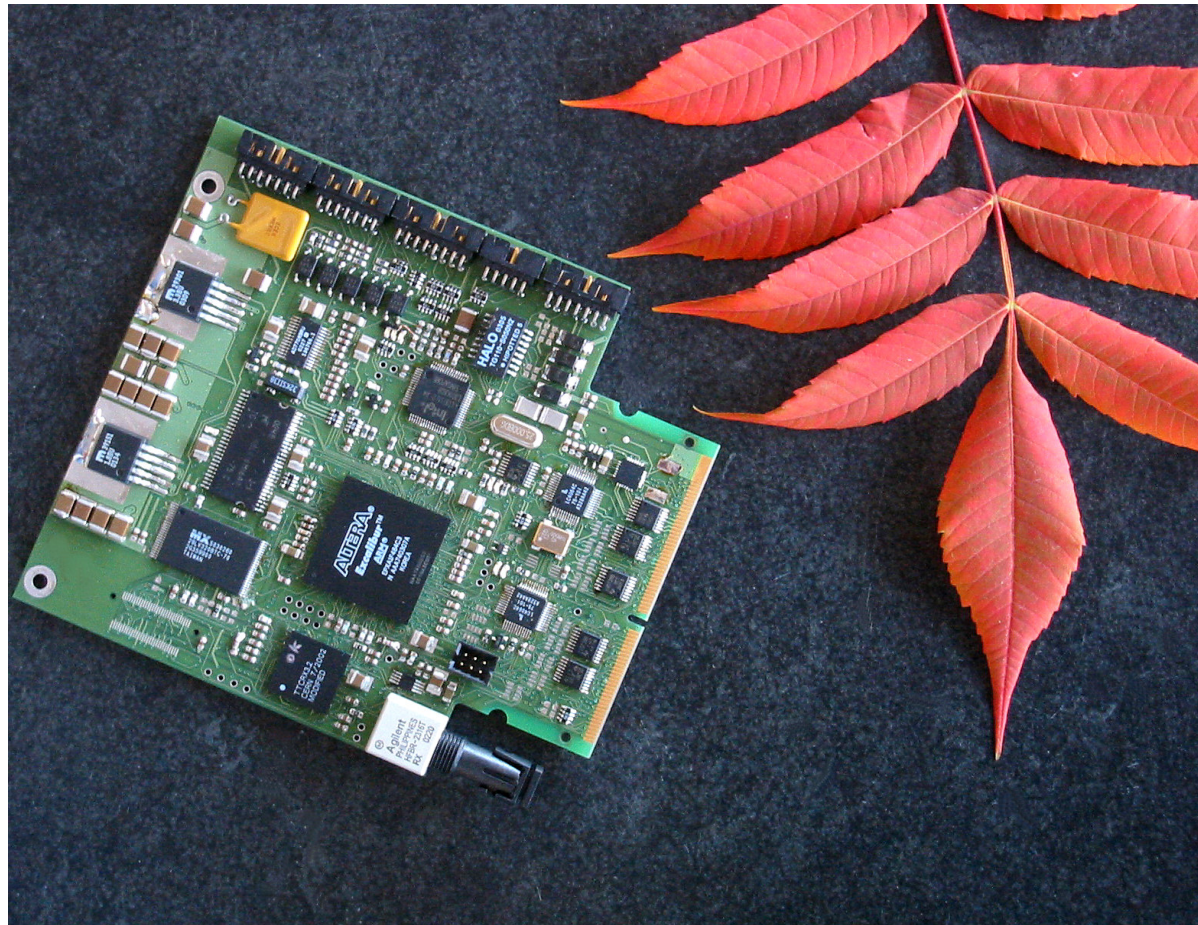
# DCS Board Production Readiness Review

January 2004

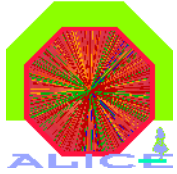
Project Link : <http://www.kip.uni-heidelberg.de/ti/DCS-Board/current/>

page 1

Board Version 1.16  
Sept./ Oct. 2003



Dirk Gottschalk  
Holger Höbbel  
Volker Kiworra  
Tobias Krawutschke  
Volker Lindenstruth  
Stefan Martens  
Vojtech Petracek  
Marc R. Stockmeier  
Heinz Tilsner



# DCS Board Production Readiness Review

Page 2

## Content

DCS board requirements

Overview

Operating Conditions

Basic Functional Tests

Basic Electrical Tests

Radiation Testresults

Error Handling

Status

Known Issues and Changes

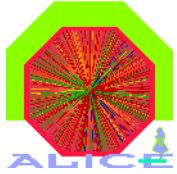
Schematics prototype version 1.16 / revised version 1.51

Bill of Material version 1.16 (plain text)

Layout prototype version 1.16 (zipped pdf)

Cost ( Not public. See confidential appendix document )

Supplier List (plain text. Not public. See confidential appendix document )



# DCS Board Production Readiness Review

Page 3

## DCS Board Requirements for ALICE TRD :

Clock distribution for MCM modules

Control of MCMs via LVDS connections

JTAG programming features for reconfiguration

JTAG master capability for adjacent neighborhood revitalisation

ADCs for voltage and temperature monitoring

Magneticless Ethernet for magnetic field applications

Control of 24 voltage regulators on Readout Boards

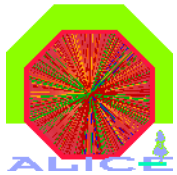
Clock recovery from optical link via TTCrx

Separat PLL design for FPGA independent clock availability while reboot  
or reconfiguration

Common I/Os for user specific configuration

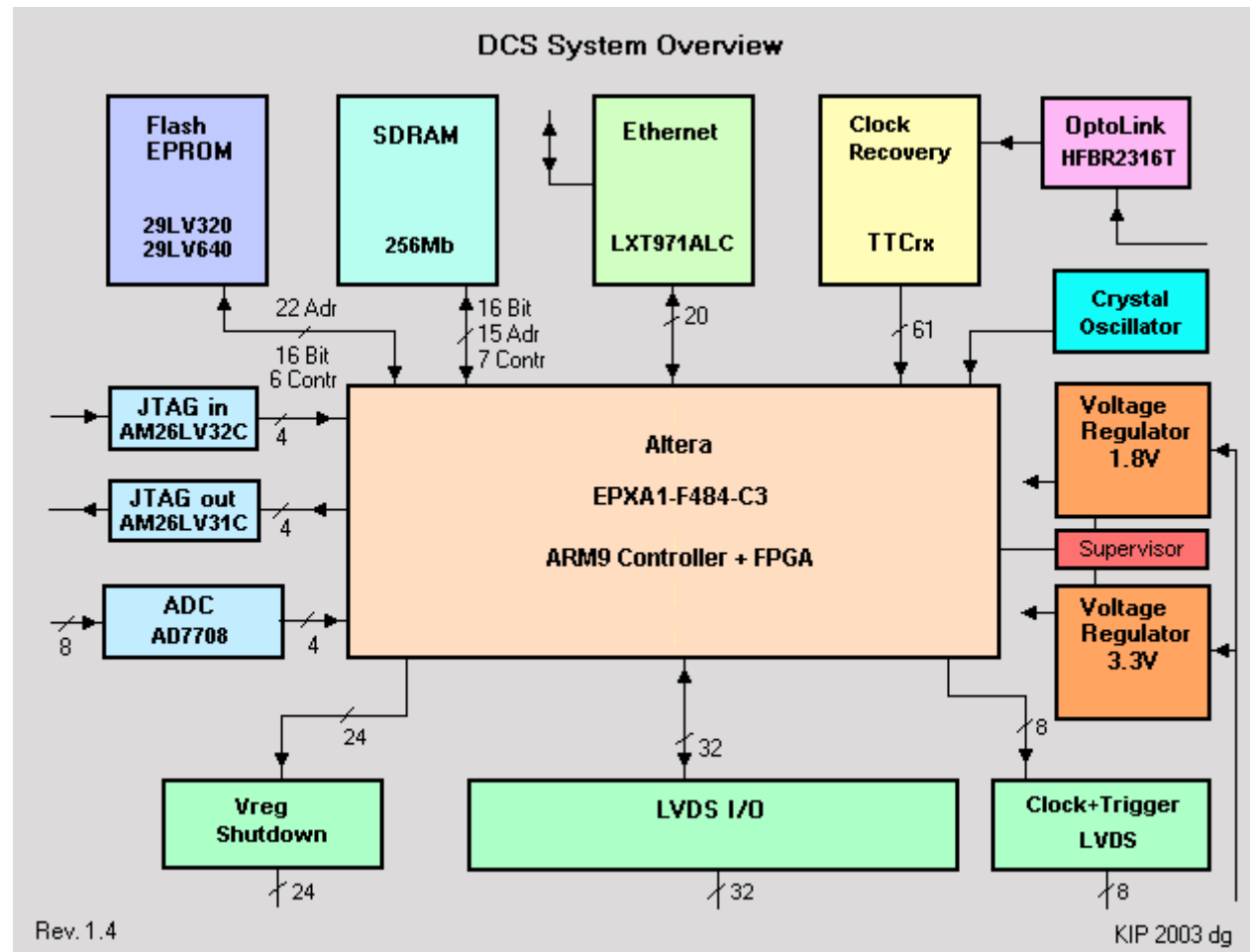
256MBit min. SDRAM and 32MBit min. Flash EPROM

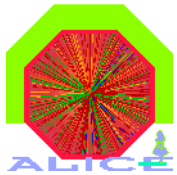
Maximum mechanical height : 16 mm incl. ROB



# DCS Board Production Readiness Review

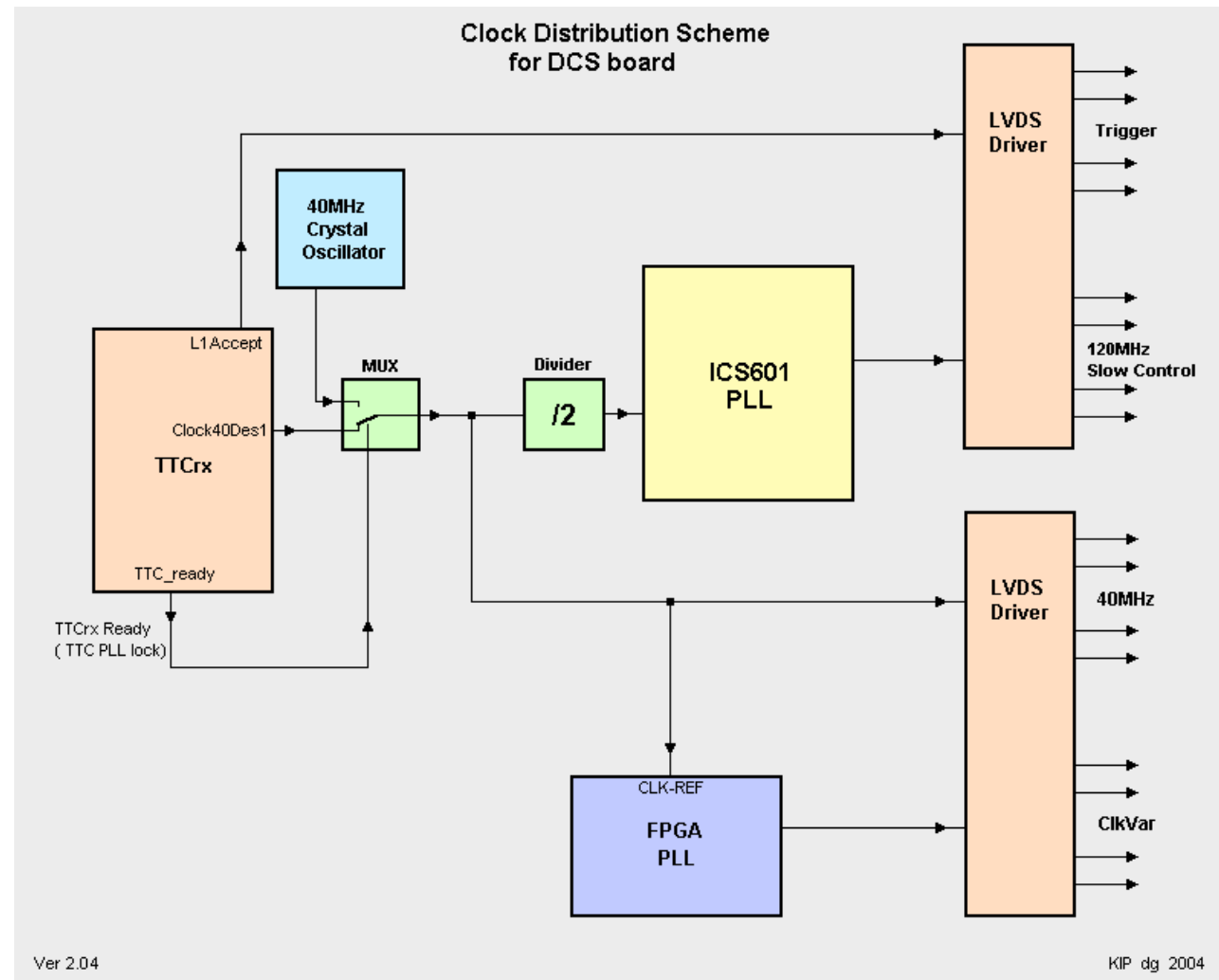
DCS board schematic overview.

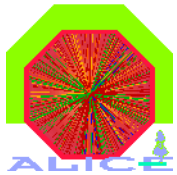




# DCS Board Production Readiness Review

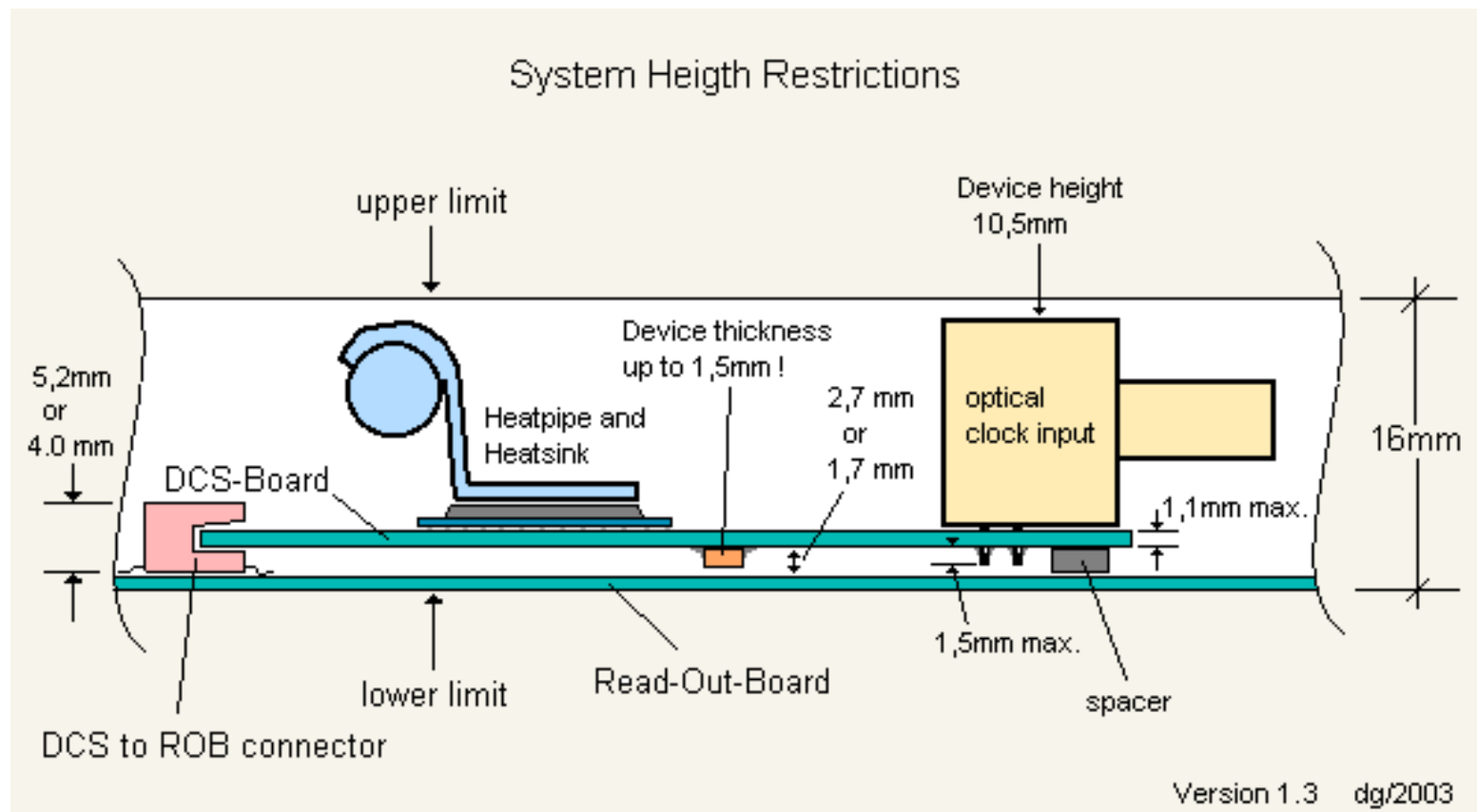
DCS board clock distribution.

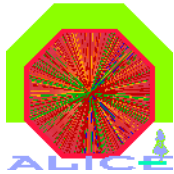




# DCS Board Production Readiness Review

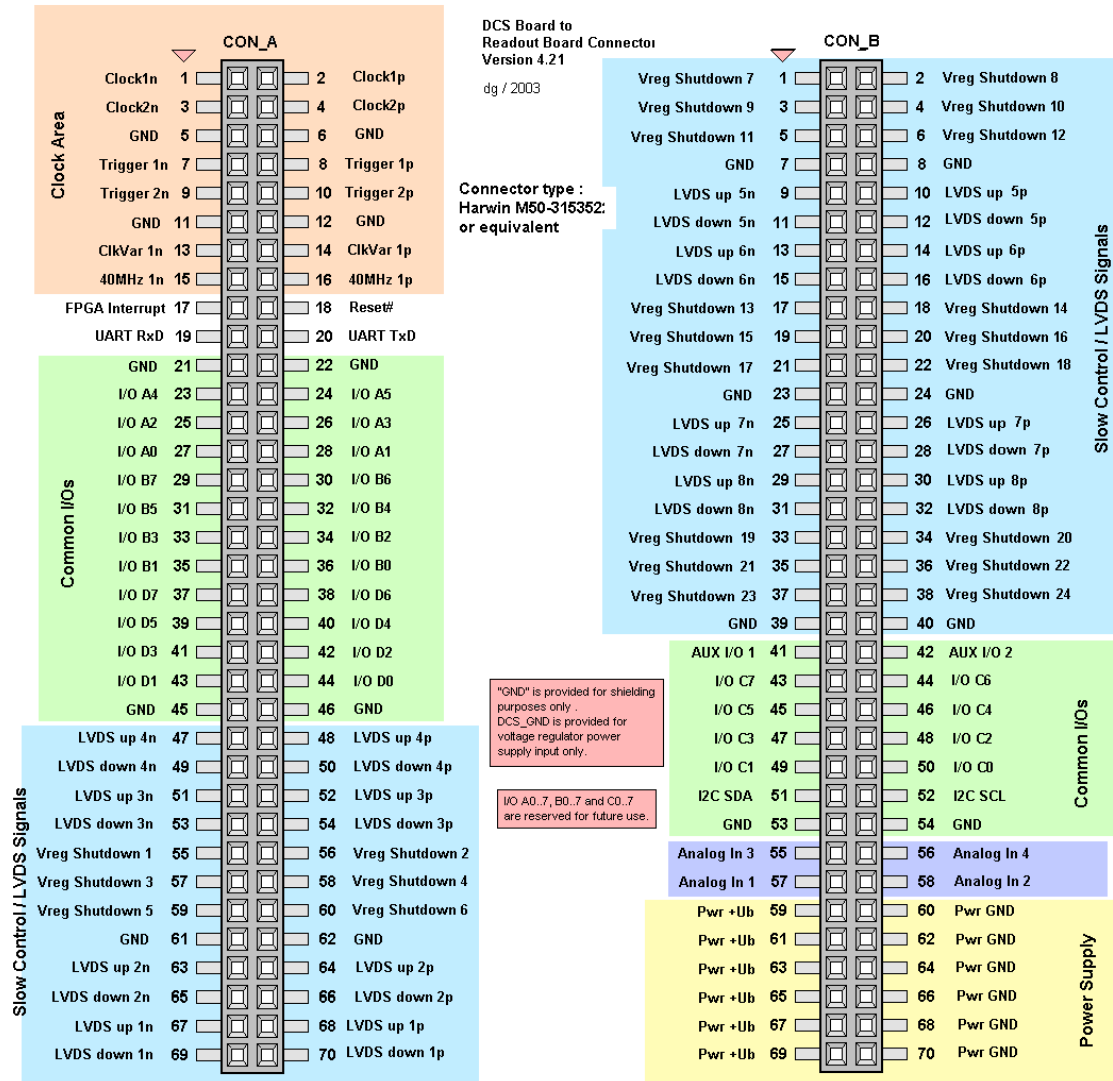
DCS board mechanical  
hight view on Readout Board.

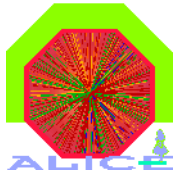




# DCS Board Production Readiness Review

DCS board connector pinout.



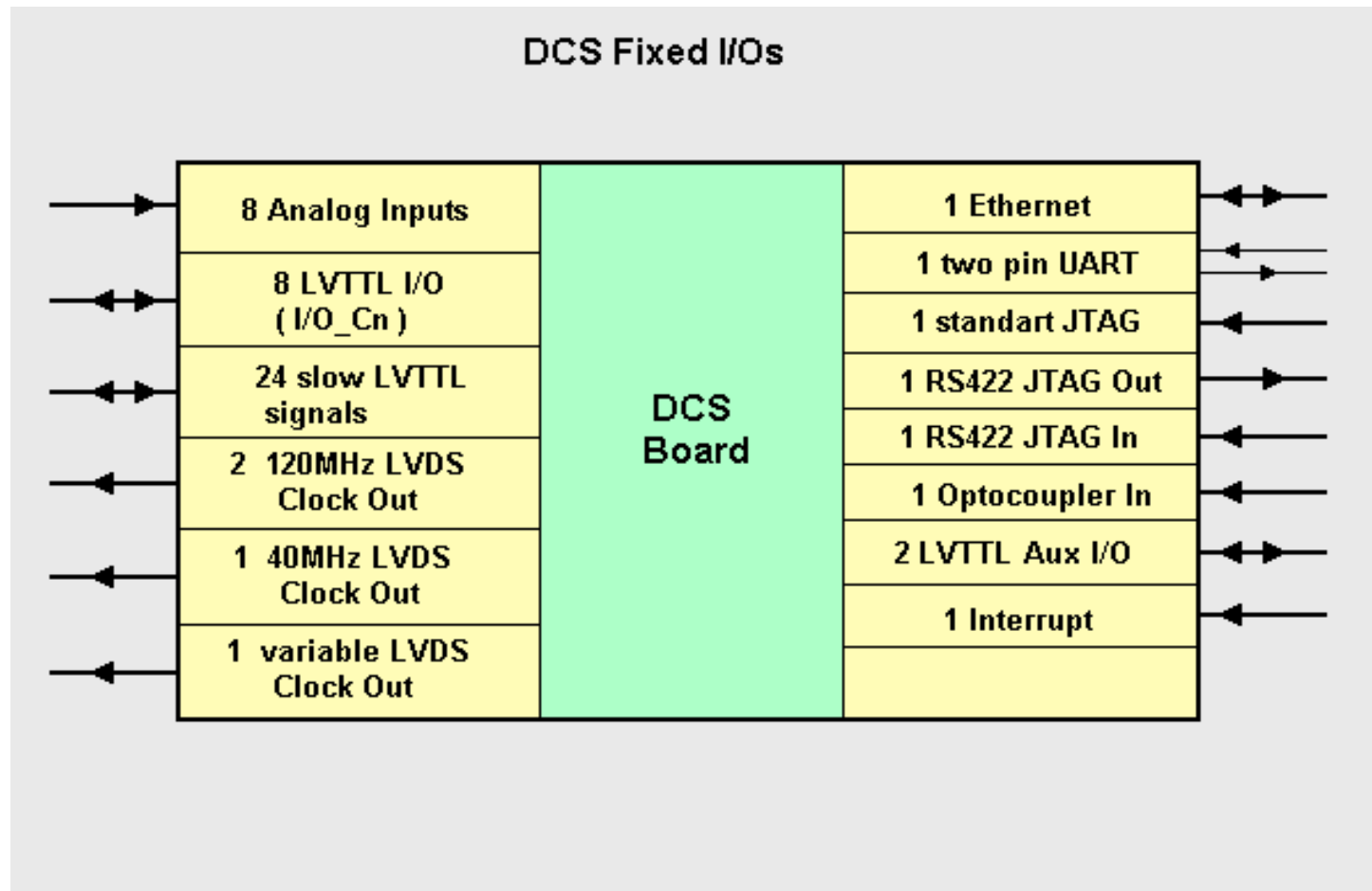


# DCS Board Production Readiness Review

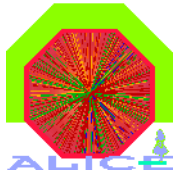
DCS board I/O Configuration Options.

Page 8

Fixed I/Os :



D.Gottschalk

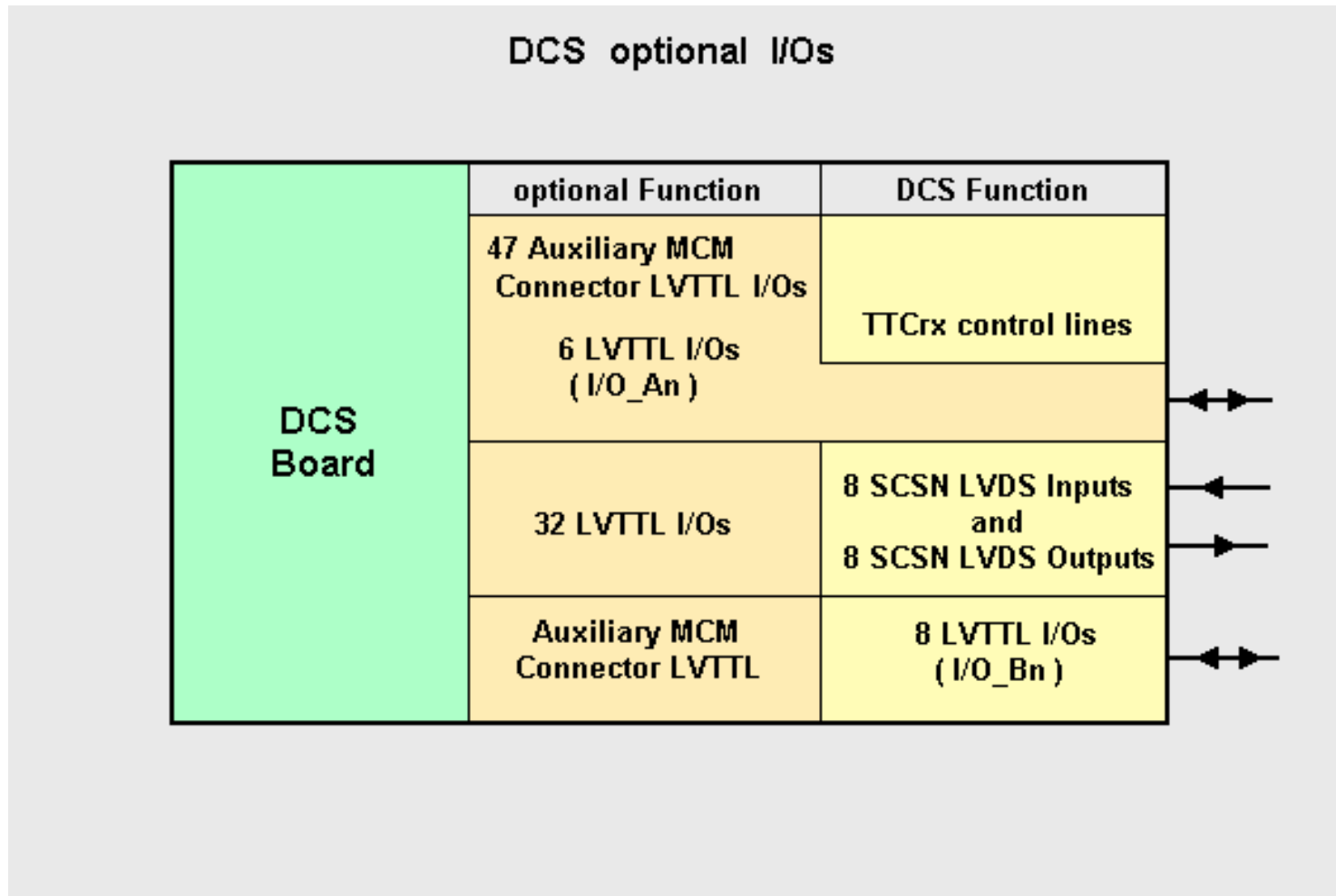


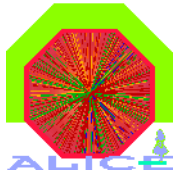
# DCS Board Production Readiness Review

DCS board I/O Configuration Options.

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Fixed I/Os :

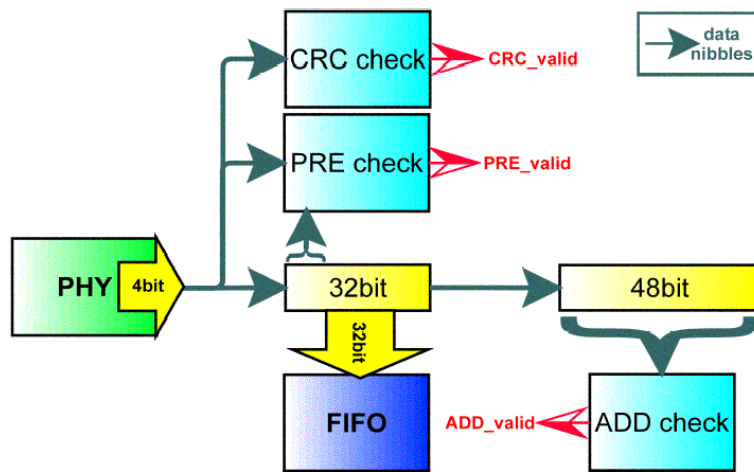




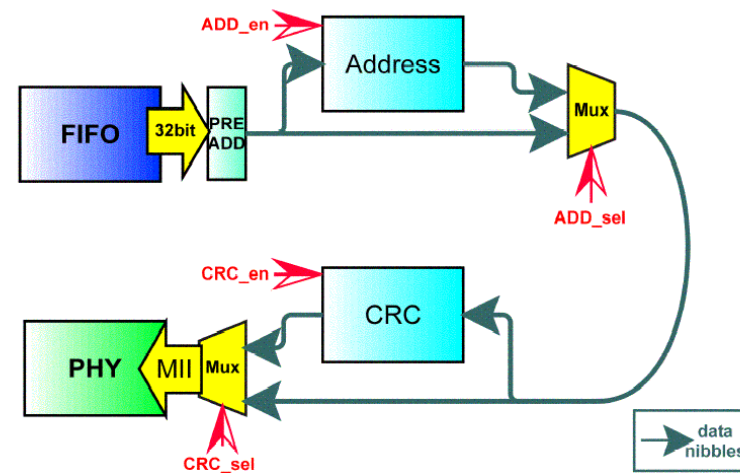
# DCS Board Production Readiness Review

DCS board ethernet concept :

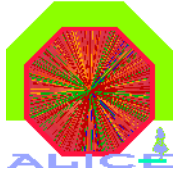
Contains Easynet FPGA design as MAC and a magneticless solution with an opamp driver for magnetic field applications.



data flow chart of the E<sub>4</sub>SYNET M<sub>4</sub>C receiver



data flow chart of the E<sub>4</sub>SYNET M<sub>4</sub>C sender



# DCS Board Production Readiness Review

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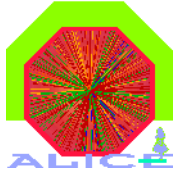
## Operating Conditions :

Input Voltage : 3,8 .. 4,2 V ( tested down to 3,3V with Linux still responding.)

Temperature : +15 ... +25 °C

Current Consumption : ~ 900mA

Power Dissipation : ~ 3,6W at 4Volt



# DCS Board Production Readiness Review

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## Basic Functional Tests :

Voltages : okay

ARM and FPGA : okay

standart JTAG : okay

DCS special JTAG : tbd

Memory : up to 135MHz okay / 120MHz guaranteed

Flash EPROM : okay

Vreg Shutdown CPLD : tbd ( no problems expected / clock distribution CPLD worked well )

ADC : okay

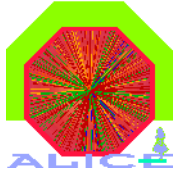
LVDS / SCSN : okay

Ethernet ( with and without transformer ) : 10MBit okay, 100MBit okay but not guaranteed

TTCCrx : okay ( Configuration with FPGA tested by T. Alt at Bergen/Norway )

Optolink : okay

Optocouplers : okay



# DCS Board Production Readiness Review

Page 13

## Basic Electrical Tests :

Voltages : Noise/Ripple below 80mV with Linux booting, idle below 20mV  
Linux still active down to 3.3 V power supply input.  
( 3.0 V behind voltage regulator / measured statically )

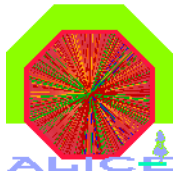
LVTTL Signals on EPXA1 and CPLDs : okay but have over/undershoot

Ethernet Link : no errors on link with 65m cable length (10MBit)  
with magneticless ethernet.

ADC Noise, Distortion, Stability : tbd

LVDS signals : okay

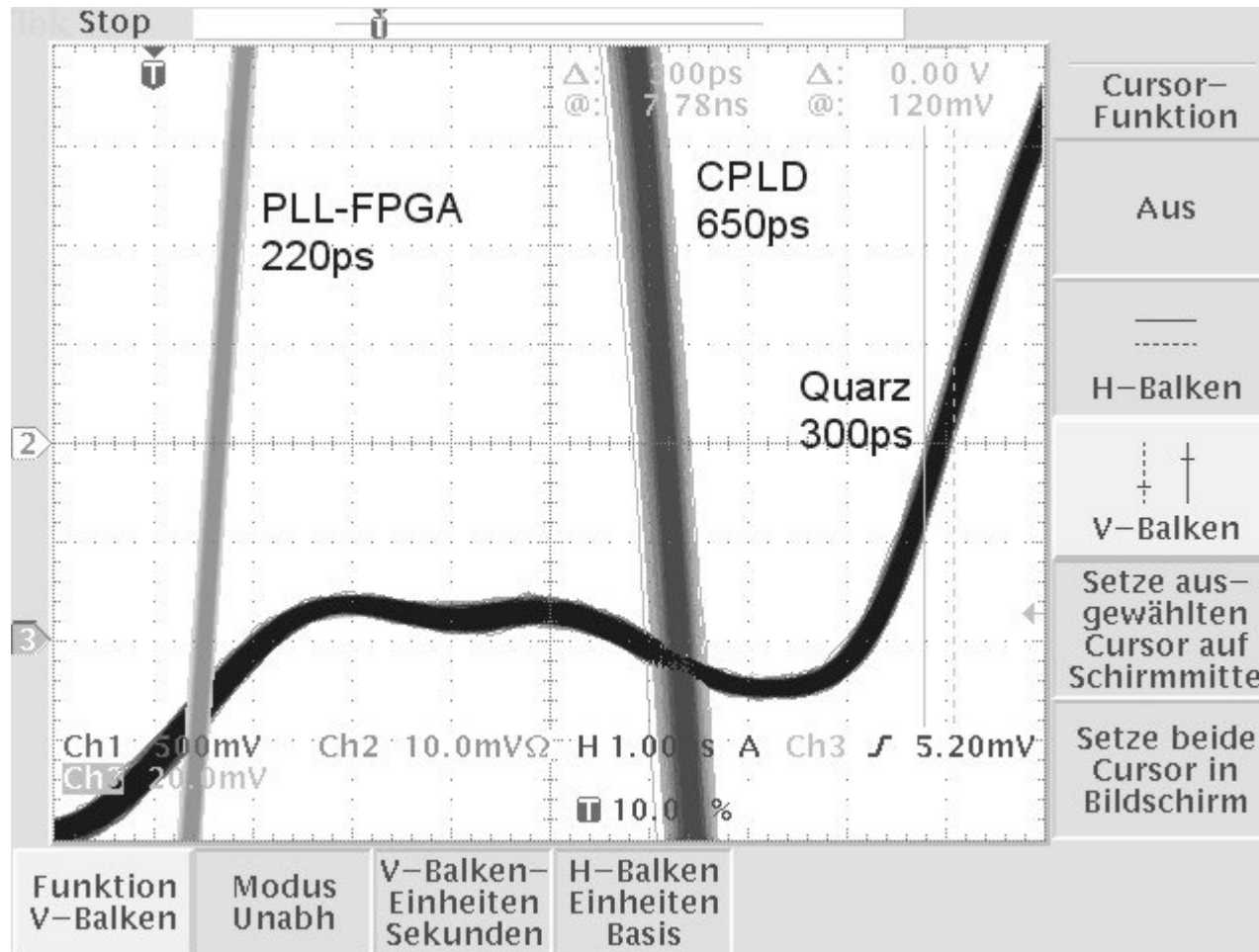
DCS board runs up to 45MHz master clock. ( =135MHz memory clock )



# DCS Board Production Readiness Review

## Jitter of FPGA PLL

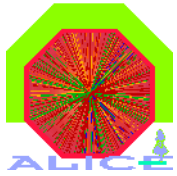
Page 14



The PLL was connected to a standard output pin on FPGA.

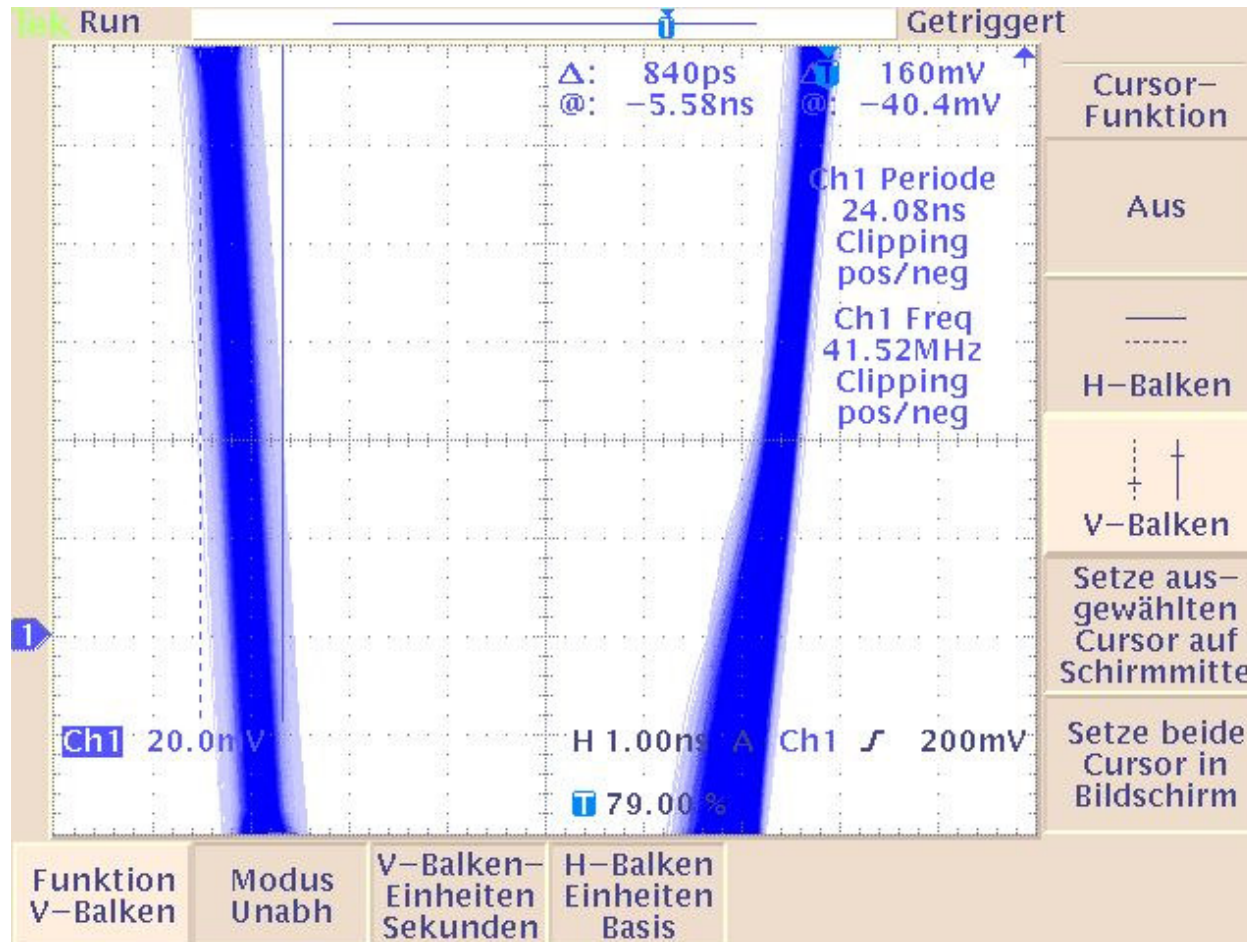
For the measurement the scope triggered on signal „PLL-FPGA“.

V. Kiworra



# DCS Board Production Readiness Review

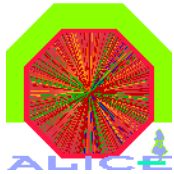
## Jitter CPLD



Jitter measurement with one logic gate in CPLD

Jitter : 840ps

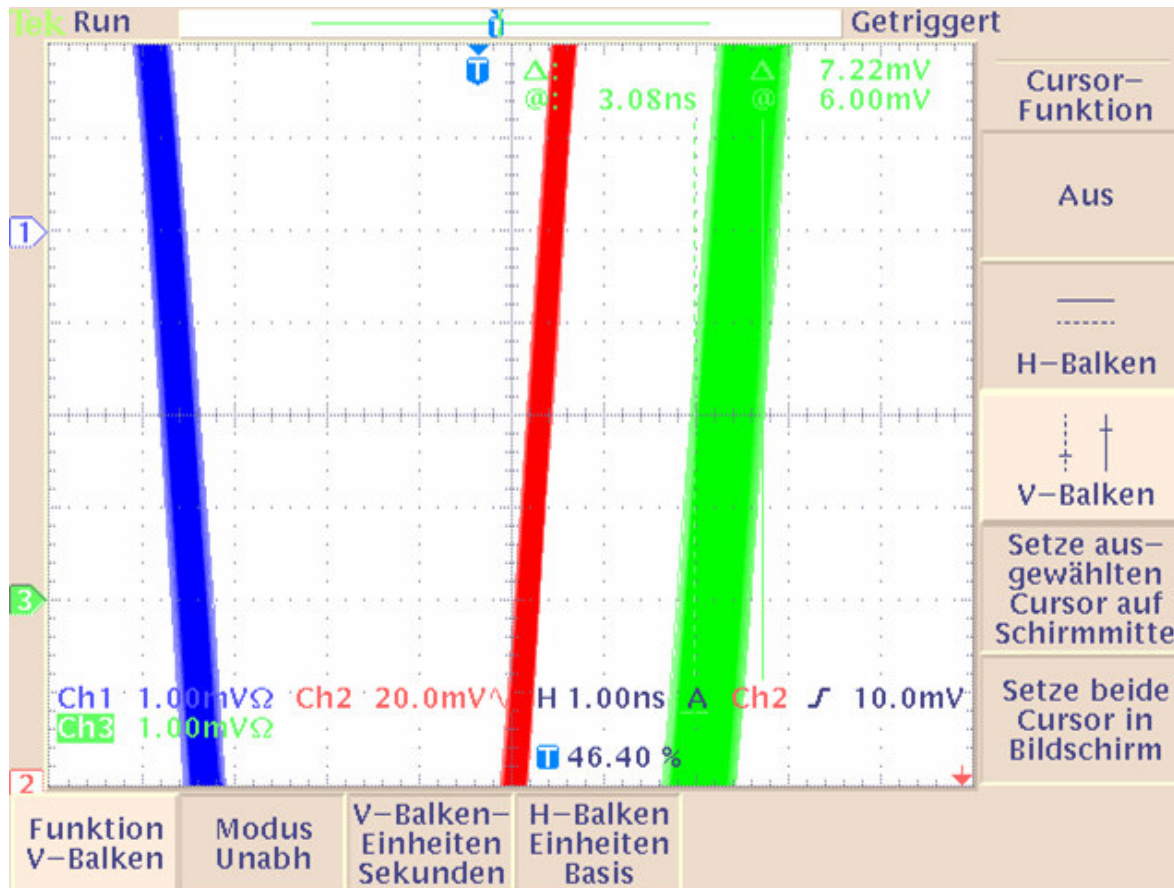
V. Kiworra



# DCS Board Production Readiness Review

Jitter measurement from TTCrx input to PLL output with ICS601

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green curve  
ICS601-01  
PLL output  
Jitter = 840ps

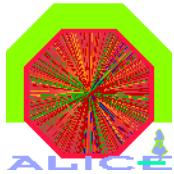
blue curve  
TTCrx input  
Jitter = 360ps

red curve  
TTCrx output  
Jitter = 280ps

Triggered on  
TTCrx output

PLL was fed by 74HCT161 counter.

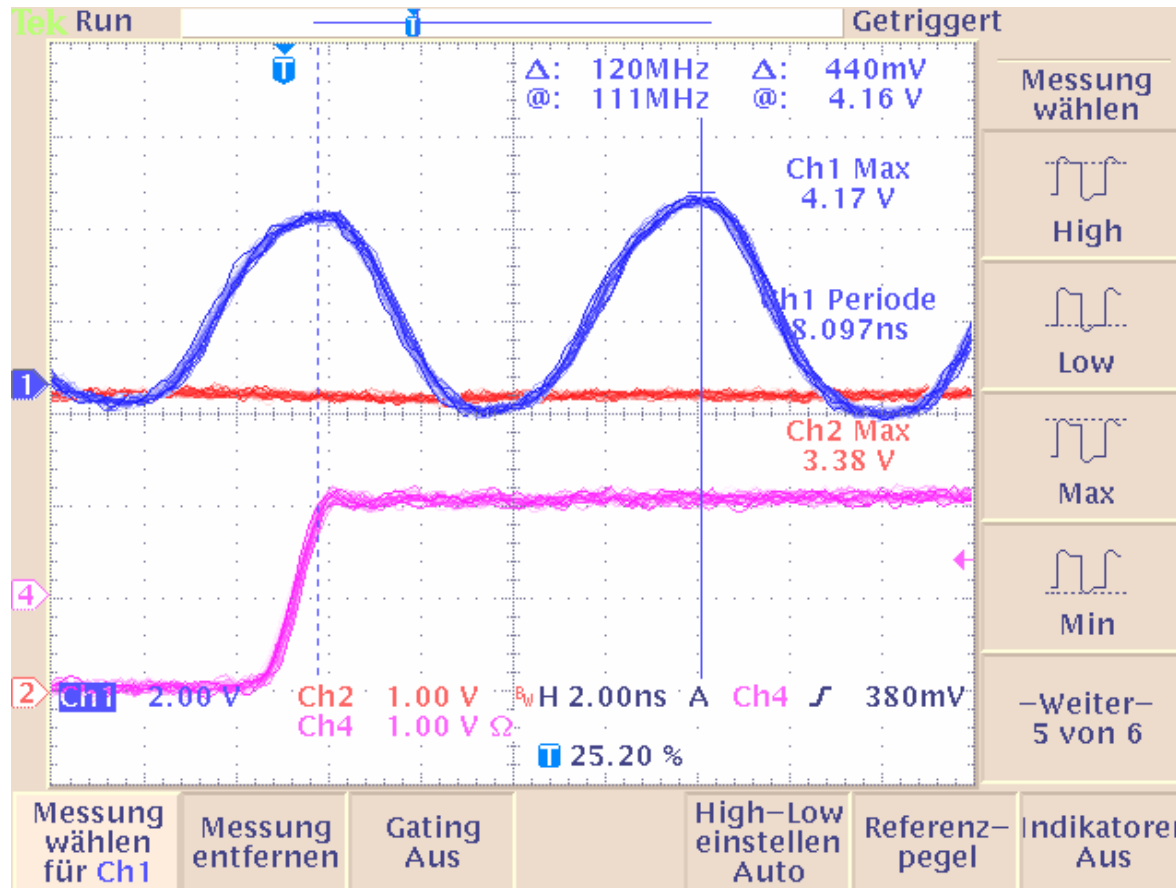
V. Kiworra



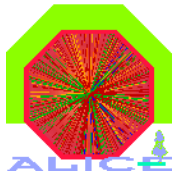
# DCS Board Production Readiness Review

Jitter measurement with ICS601 at 3,38 Volt

Page 17



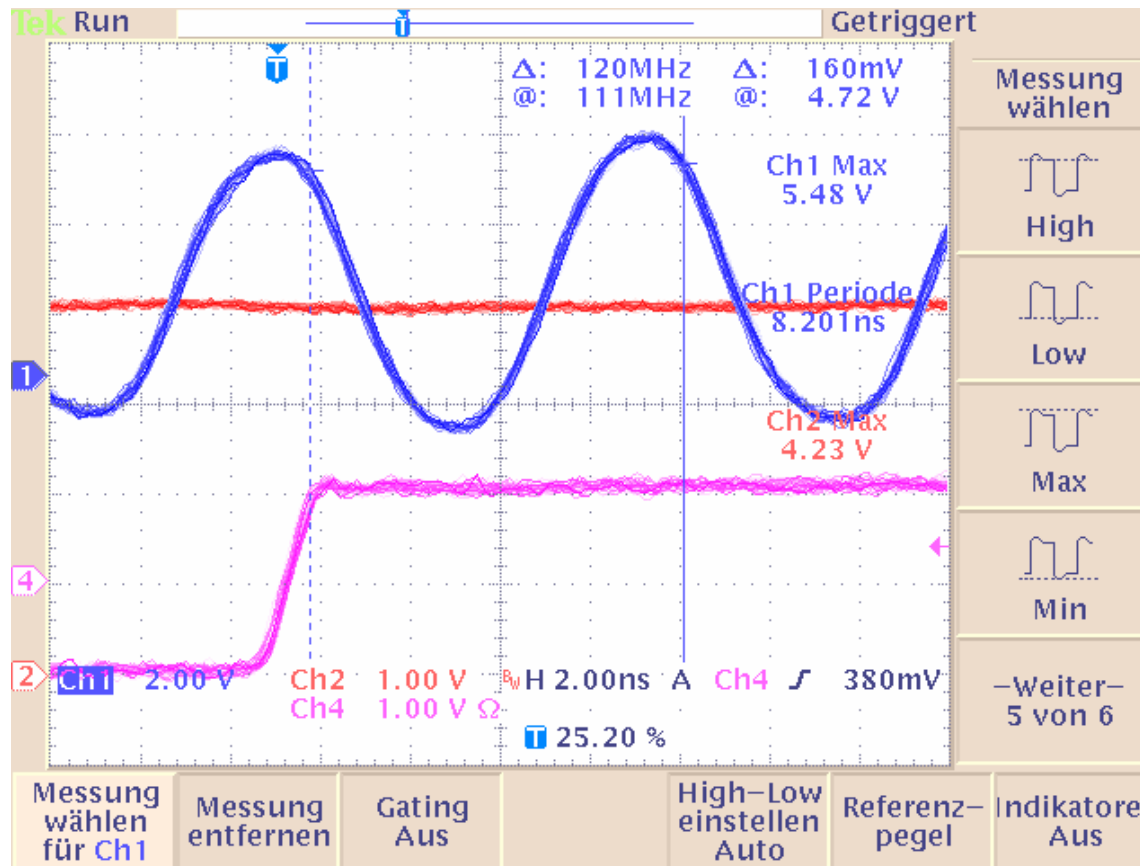
V. Kiworra



# DCS Board Production Readiness Review

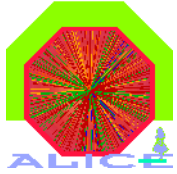
## Jitter measurement with ICS601 at 4,23 Volt

Page 18



Phase shows dependency on supply voltage. 3,3 volt supply quality will be enhanced.

V. Kiworra



# DCS Board Production Readiness Review

Radiation Beamtest

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## Assumption of total radiation dose for ALICE TPC

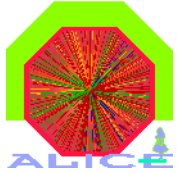
$6 \times 10^9$  particles ( n,p,Pi,K ) in 10 ALICE years per  $1\text{cm}^2$   
with

$6 \times 10^8$  protons

$3,5 \times 10^9$  pions and kaons

$1,9 \times 10^9$  neutrons

( Source : TPC meeting October 2003 )



# DCS Board Production Readiness Review

Radiation Beamtest Results (1) :

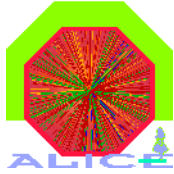
Page 20

Device Type	Device Name	Manufact.	Partikels	Results	by / at
FPGA	EPXA1F484-C3	Altera	Protons	see plots below	1*)
ARM Core	EPXA1F484-C3	Altera	Protons	see plots below	1*)
Flash EPROM	MX29LV320BTC-70	Macronix	Protons	see plots below	1*)
SDRAM	MT48LC16C16A2	Micron	Protons	see plots below	1*)
CPLDs	LC4032ZC-75T48	Lattice	Protons	see results below	1*)
Ethernet Phy	LXT971ALC	Intel	Protons	see results below	1*)
ADC	AD7708BRU	AD	Protons	see plots below	1*)
Optocouplers	LTV357T	Liteon	Protons	see results below	1*)
Voltage Ref.	AD1582ART	AD	tbd		
Charge Pump	REG711EA-5	BB/TI	tbd		
LVDS Driver	SN75LVDT390PW	TI	Protons	see results below	1*)
LVDS Receiv.	SN75LVDS391PW	TI	Protons	see results below	1*)

\*1) D. Gottschalk/KIP, S. Martens/KIP, M. Stockmeier/PI, P. Struck/KIP, H. Tilsner/KIP at University of OSLO November 2003

\*2) L. Musa / CERN made rad tests as well at CERN and University of OSLO.

\*3) Links provide documents for details.



# DCS Board Production Readiness Review

## Radiation Beamtest Results (2) :

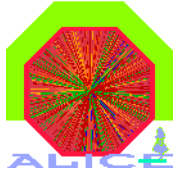
Page 21

Device Type	Device Name	Manufact.	Partikels	Results *3)	by / at
RS422 Driver	AM26LV31C	TI	tbd		
RS422 Receiv.	AM26LV32C	TI	tbd		
Watchdog	TPS3306-18DGK	TI	tbd		
Voltage 3V3	MIC29301-3.3BU or LP3962ES-3.3	Micrel NS	Protons	see plots below	/ *2)
Voltage 1V8	MIC39151-1.8BU or LP3962ES-1.8	Micrel NS	Protons	see plots below	/ *2)
Optolink	TRR-1B43	Truelight	Protons, Gamma, Neutrons	<a href="#">Okay / doc.pdf</a>	Gastal / Moreira / CERN
Optolink	HFBR-2316T	Agilent	Protons, Gamma, Neutrons	<a href="#">Okay / doc.pdf</a>	Gastal / Moreira/ CERN
PLL					
Clock Recovery	TTCrx 3.2	CERN	??	okay	/ CERN

\*1) D. Gottschalk/KIP, S. Martens/KIP, M. Stockmeier/PI, P. Struck/KIP, H. Tilsner/KIP at University of OSLO November 2003

\*2) L. Musa / CERN made rad tests at CERN and University of OSLO.

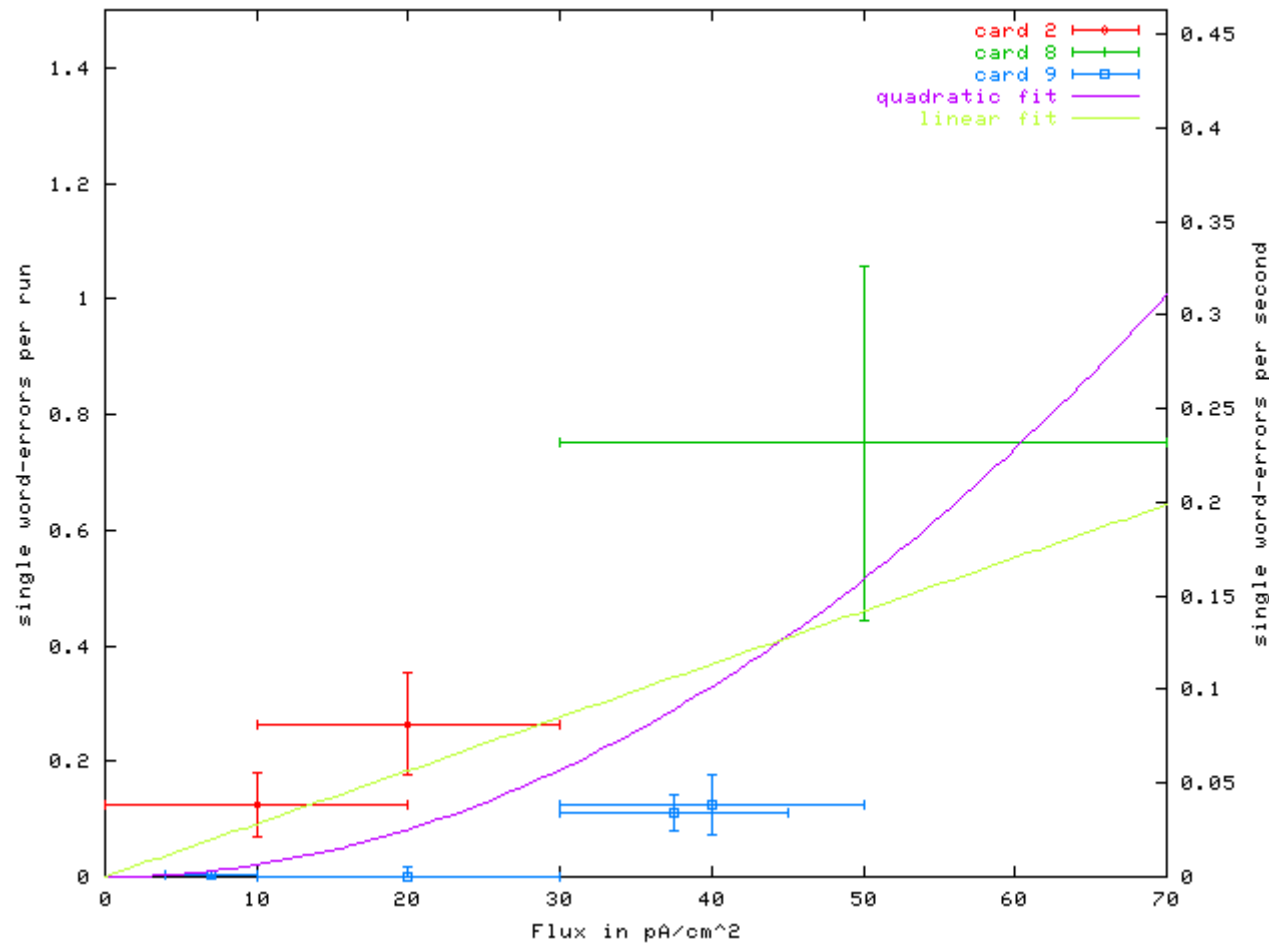
\*3) Links provide documents for details.



# DCS Board Production Readiness Review

Radiation Beamtest Plots : 256Mb SDRAM Micron MT48LC16M16

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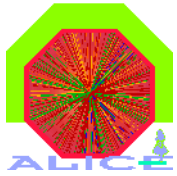
16MB used for test

Error rate :

1 error per ALICE  
year per 16MB

Test plots by  
Stephan Martens  
Diploma Thesis 2003

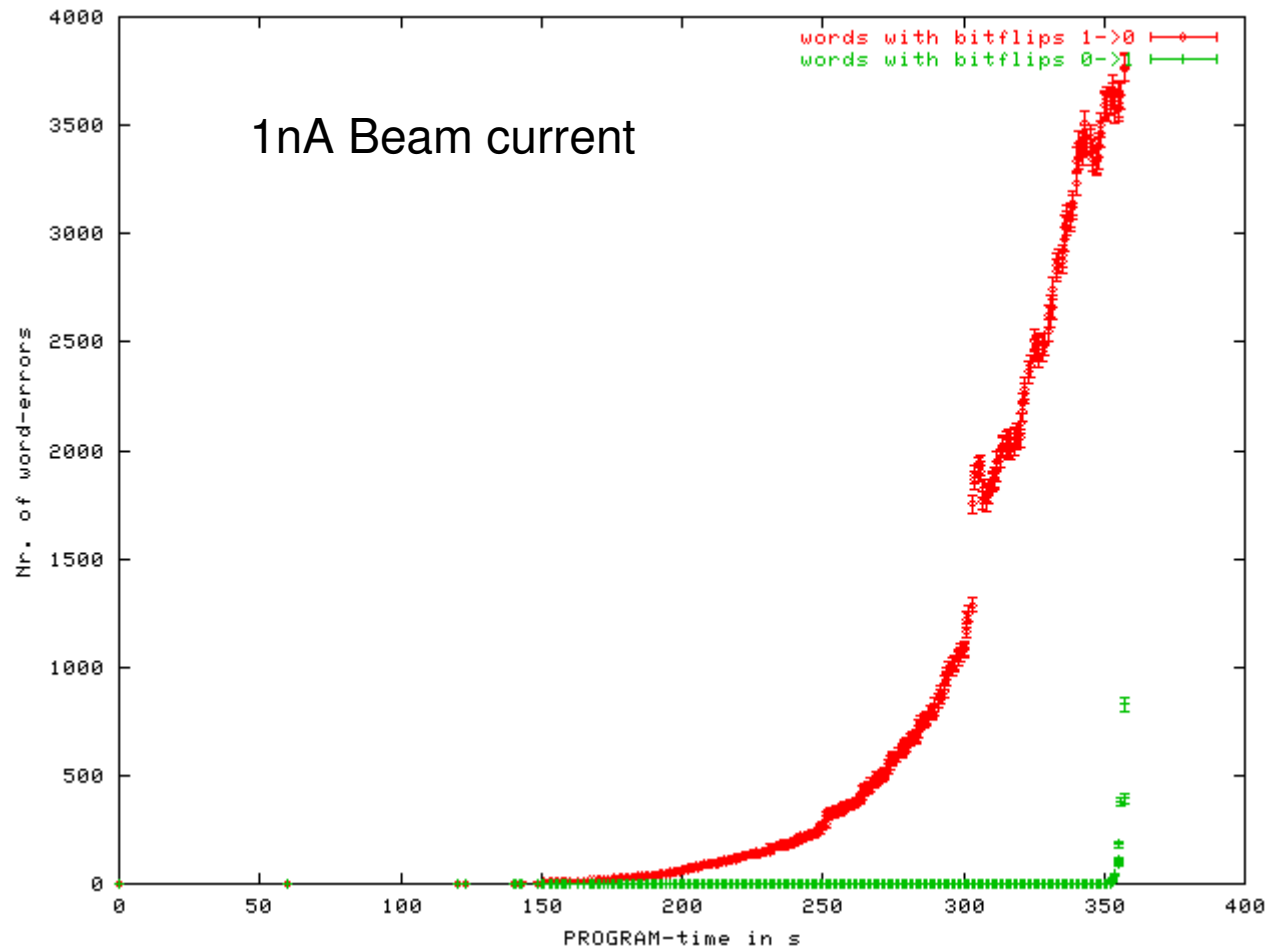
SDRAM Beam Test Plot



# DCS Board Production Readiness Review

Radiation Beamtest Plots :

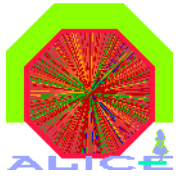
Page 23



First error after  
146 x 10 ALICE  
years

Test plots by  
Stephan Martens  
Diploma Thesis 2003

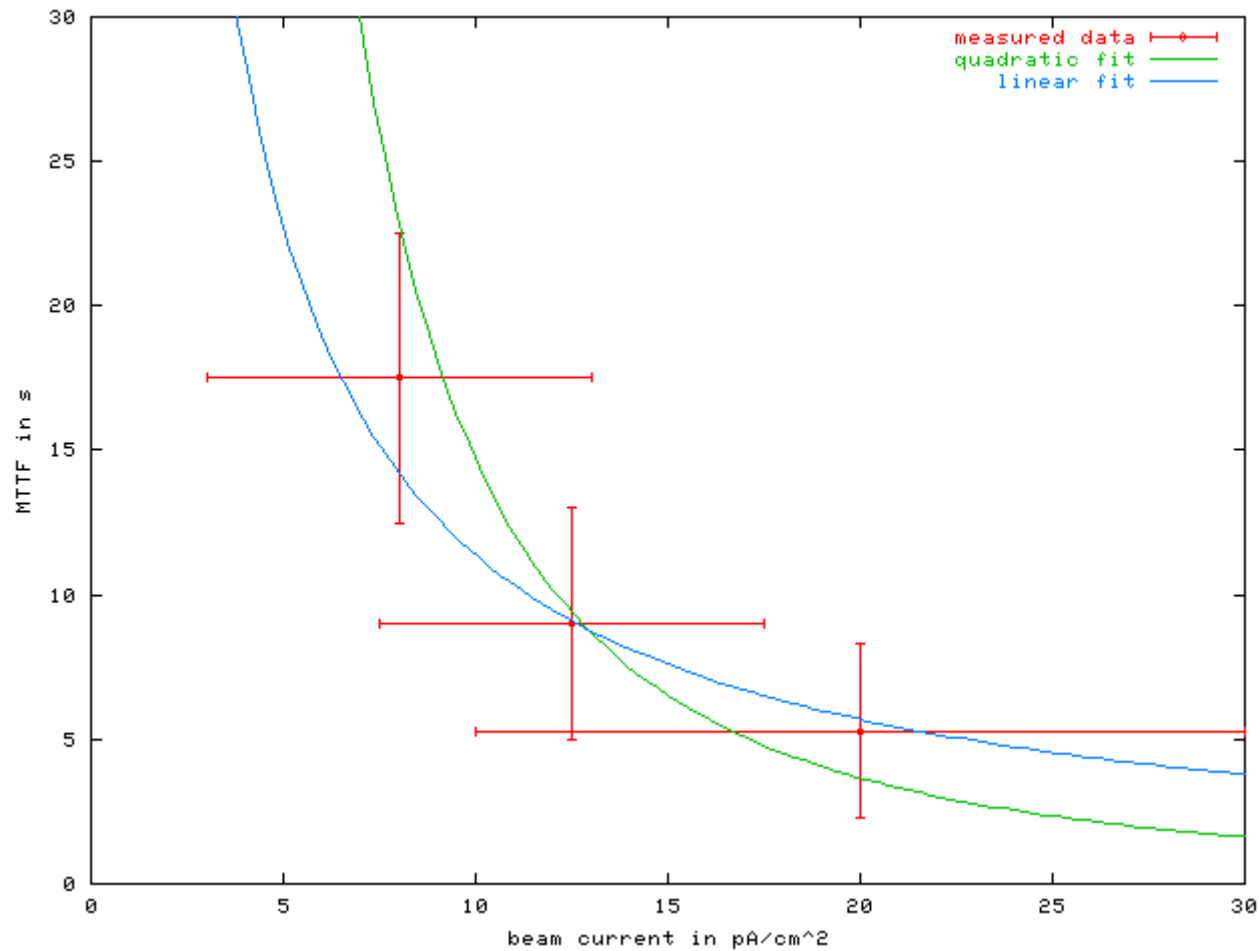
Flash EPROM Beam Test Plot



# DCS Board Production Readiness Review

## Radiation Beamtest Plots : Altera EPXA1 FPGA

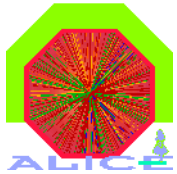
Page 24



Design :  
„Coprozessor“ with  
full FPGA usage.

Test plots by  
Stephan Martens  
Diploma Thesis 2003

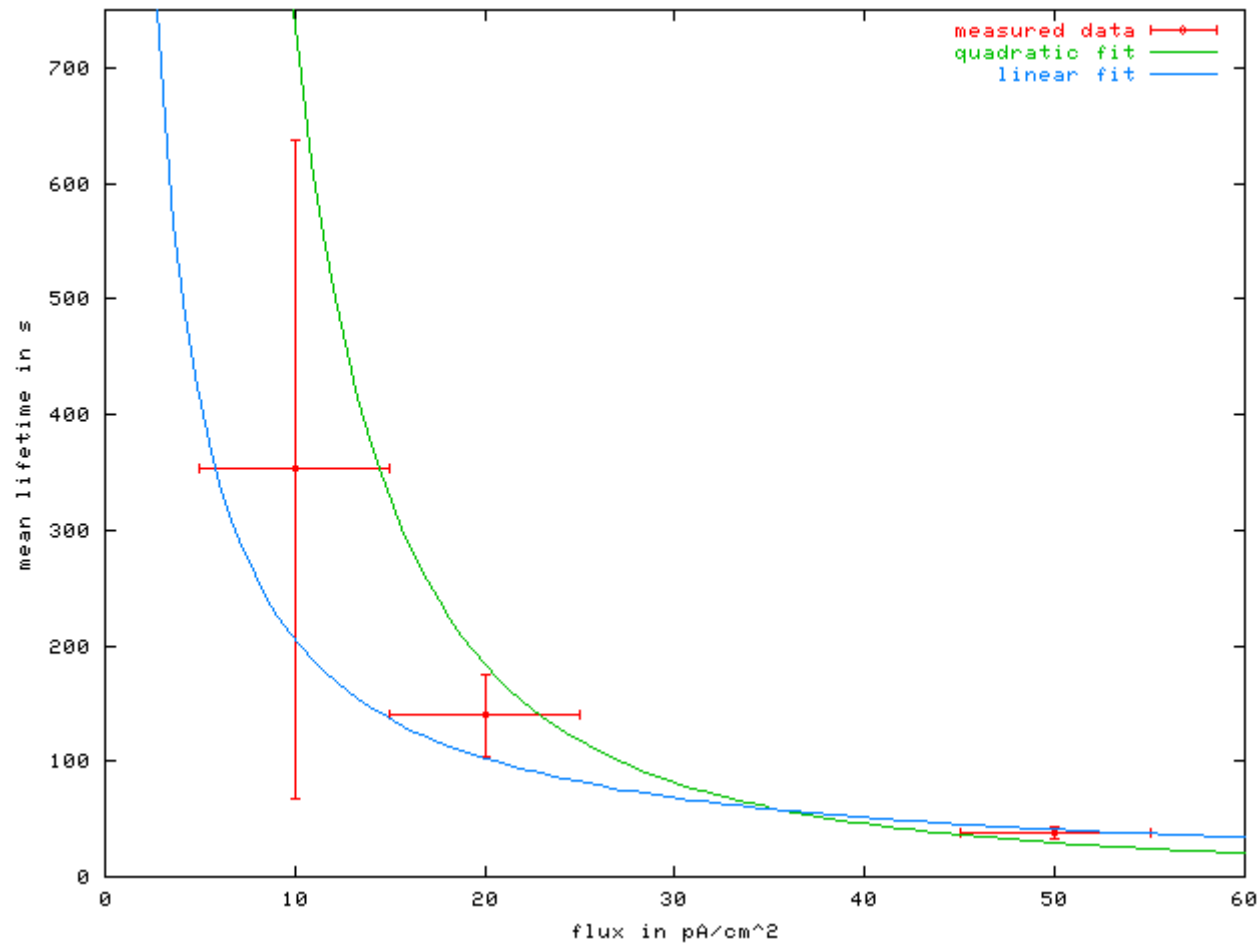
EPXA1 FPGA Beam Test Plot



# DCS Board Production Readiness Review

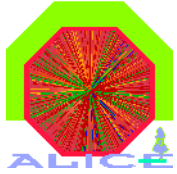
Radiation Beamtest Plots : Altera EPXA1 ARM core

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EPXA1 ARM Core Beam Test Plot

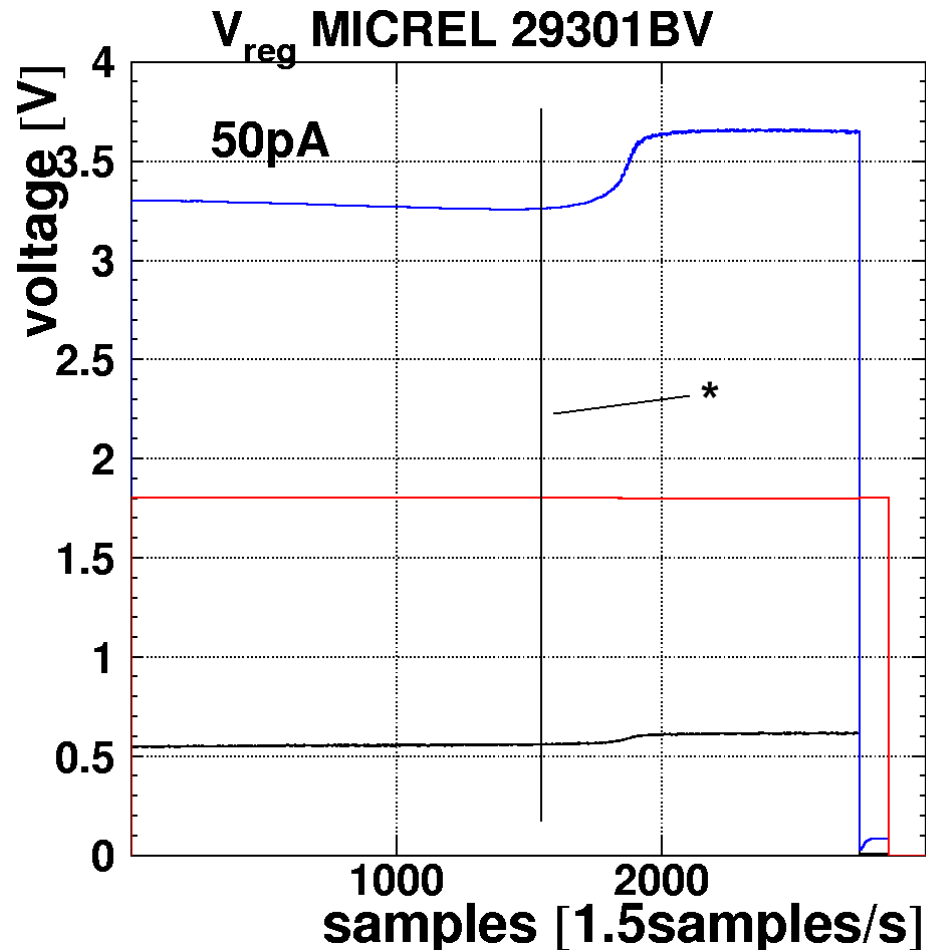
Test plots by  
Stephan Martens  
Diploma Thesis 2003



# DCS Board Production Readiness Review

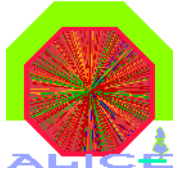
Radiation Beamtest Plots : Voltage regulators MIC29301

Page 26



\* => 55 x 10  
ALICE years

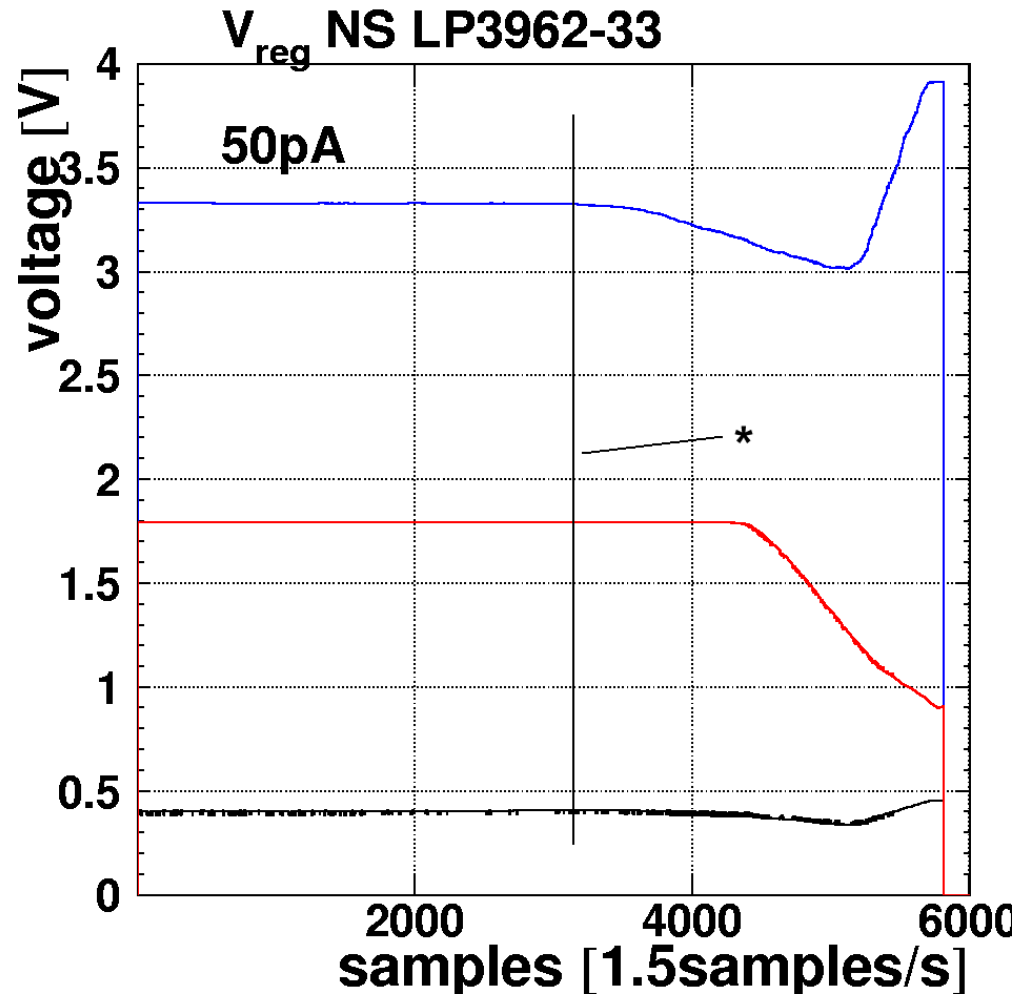
Tests by M. Stockmeier and D. Gottschalk



# DCS Board Production Readiness Review

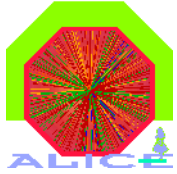
Radiation Beamtest Plots : Voltage regulator LP3962

Page 27



\* => 107 x10  
ALICE years

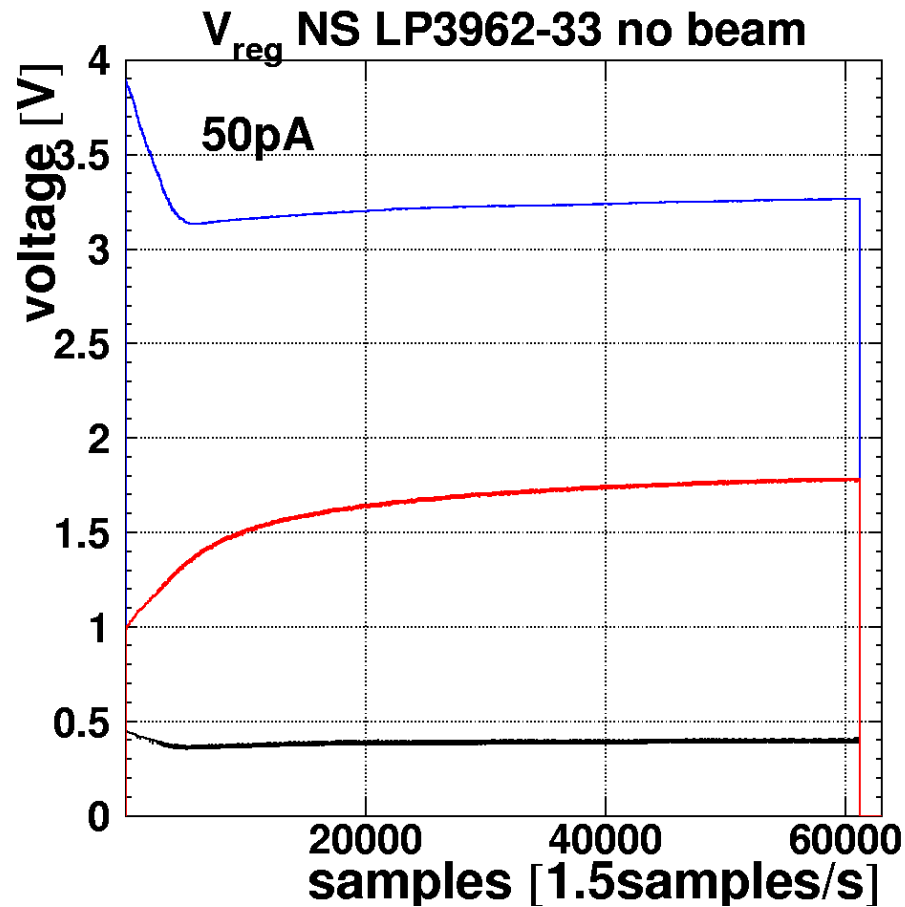
Tests by M. Stockmeier and D. Gottschalk



# DCS Board Production Readiness Review

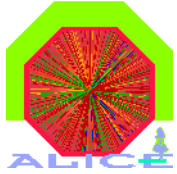
Radiation Beamtest Plots : LP3962 recovery over night

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60000 samples =>  
11 hours

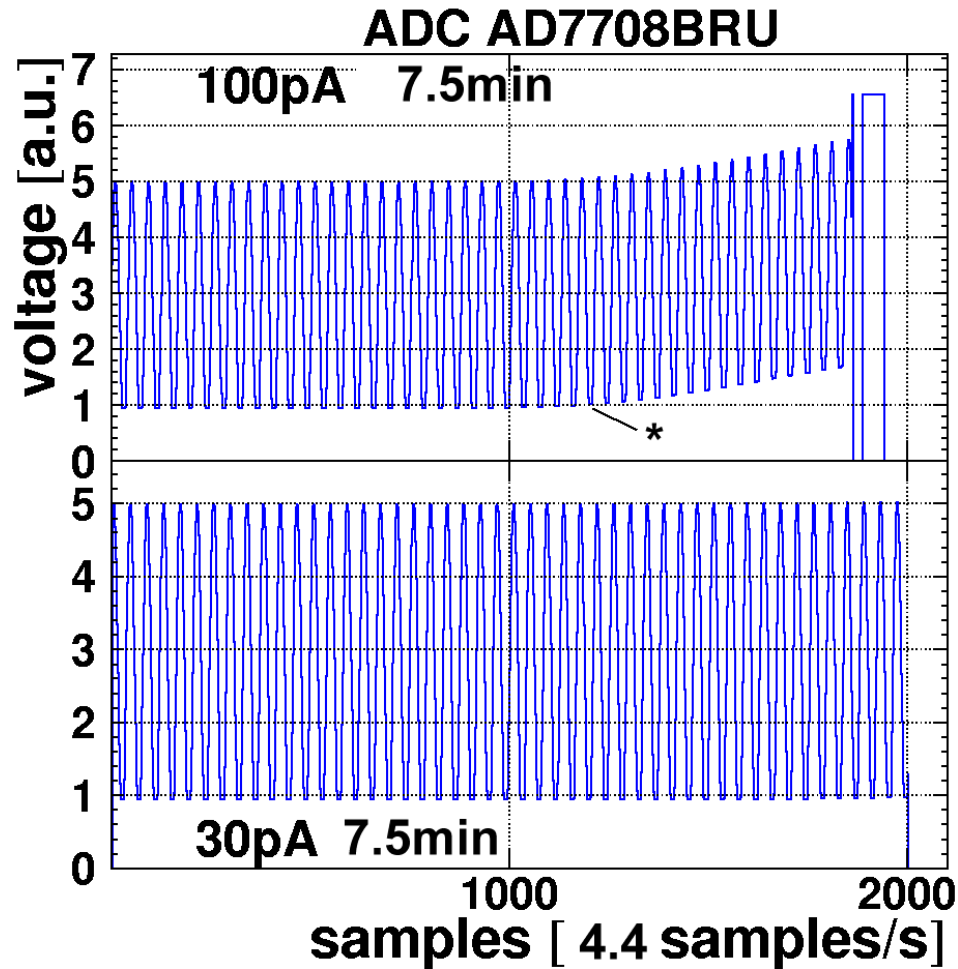
Tests by M. Stockmeier and D. Gottschalk



# DCS Board Production Readiness Review

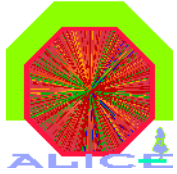
Radiation Beamtest Plots : ADC AD7708BRU

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\* is equivalent to  
90 x 10 ALICE  
years

Tests by M. Stockmeier and D. Gottschalk



# DCS Board Production Readiness Review

Radiation Beamtest : Others

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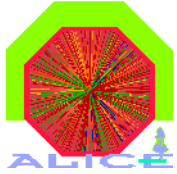
CPLD Test : at 20pA in 2421s one error at 281s  
at 50 pA in 1079s one error at 49s  
at 100pA in 741s one error at 288s  
device dead after 126 x 10 ALICE years

Tested with a twin shiftregister. Looking for nonequal values in both shifters and life activity of design.

LVDS Receiver : at 20pA in 2021s no error  
at 50pA in 2835s no error

LVDS Driver : at 20pA in 1799s no error  
equivalent to 37,5 x 10 ALICE years

Tested with SCSN design in FPGA. Looking for data packet consistency.



# DCS Board Production Readiness Review

Radiation Beamtest : Others

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Optocoupler : 20pA 30min 2.5ms pulses no effect  
50pA after 9min 12.5ms pulses dead  
100pA after 15min 12.5ms pulses dead  
no pulse inversion occurred

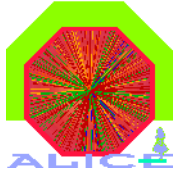
Tested with rectangular pulses looking for erroneous puls inversions or dead.

Ethernet Phy : 20pA >40min no errors  
equivalent to 50 x 10 ALICE years

Tested with connection to a PC. Looking for lost or corrupted data packets.

Ethernet driver Opamp : 20pA >40 min no errors  
equivalent to 50 x 10 ALICE years

Tested with connection to a PC. Looking for lost or corrupted data packets.



# DCS Board Production Readiness Review

Radiation Beamtest : Results

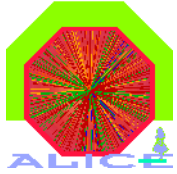
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Results where quite encouraging.

We found no „No go“.

With some devices self-healing was observed.

Mean time to failure is : 21 days for one DCS board



# DCS Board Production Readiness Review

Error Handling :

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Adjacent neighbourhood revitalisation over RS422 JTAG is provided for serious DCS board failure.

SCSN rings are redundant.

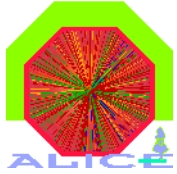
Monitoring of supply voltages and temperature is provided.

Voltage regulators can be disabled if unrecoverable short circuits occur.

Essential software could be stored multiple in Flash Memory for detection of code consistency.

Flash can be reprogrammed by adjacent DCS board.

Periodic reboots may ensure clean work.



# DCS Board Production Readiness Review

Page 34

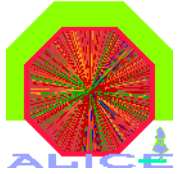
Status :

Linux is running sufficiently.

Ethernet is running in all configurations ( with transformer and with opamp driver. )

Production preparation is in progress. Industry contacts are made.

First production batch (50) expected in April/May 2004



# DCS Board Production Readiness Review

Page 35

## Known issues and changes for next revision

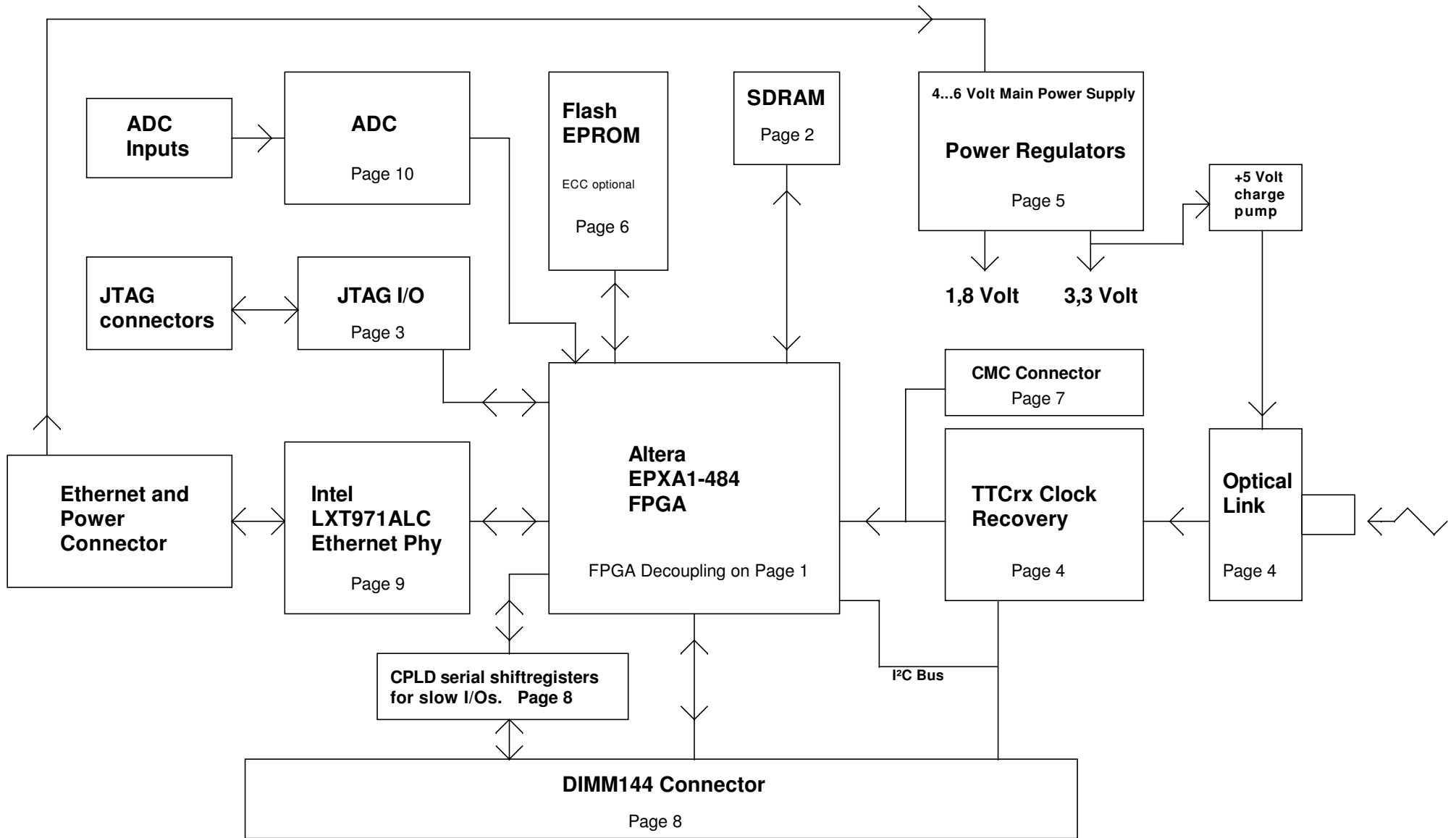
QPLL will be replaced because of high cost, unnecessary high jitter performance and high input requirements.

DIMM connector will be replaced because of mechanical forces in ROB and DCS board

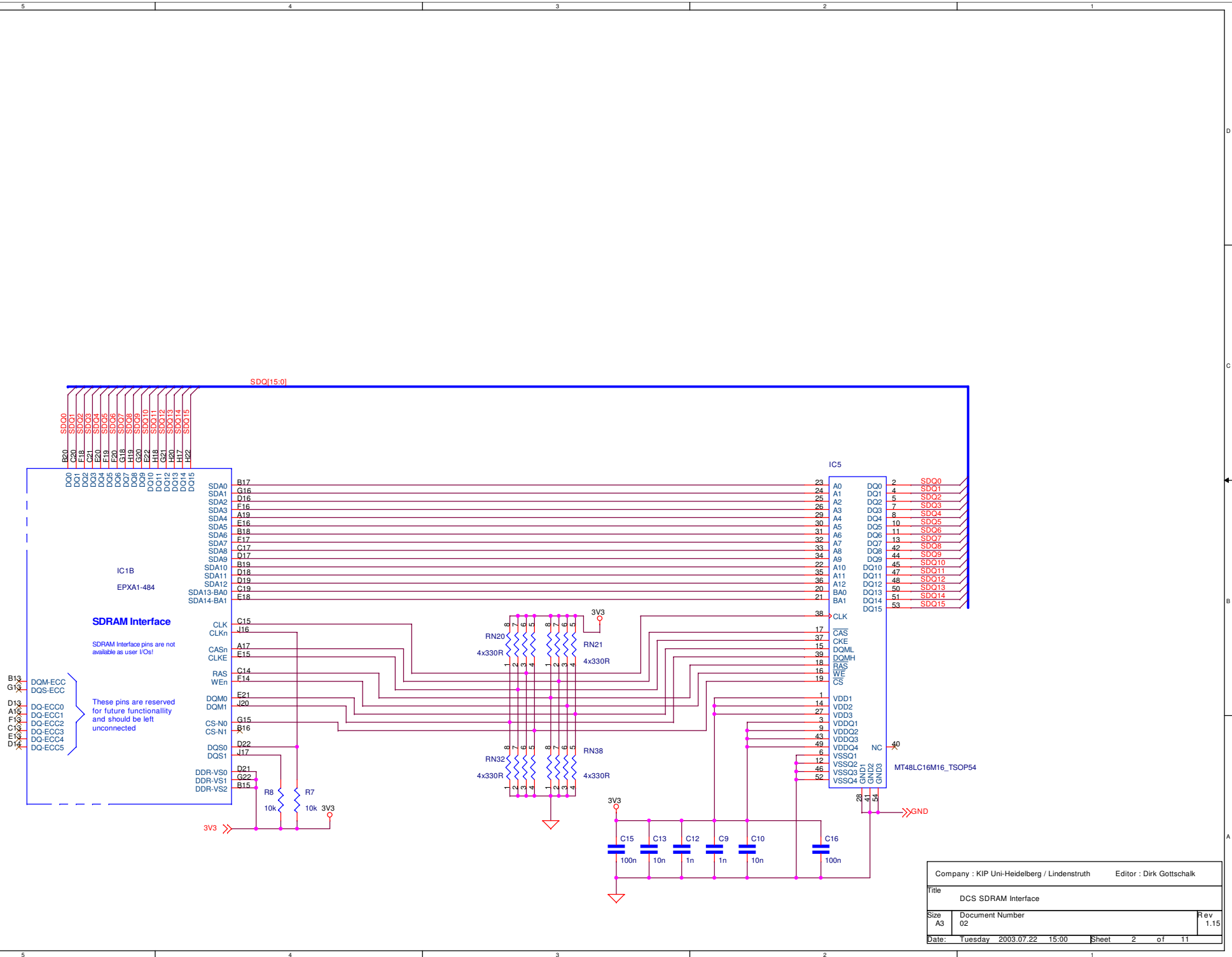
1V8 Voltage regulator will be fed by 3V3 Regulator

minor errors fixed

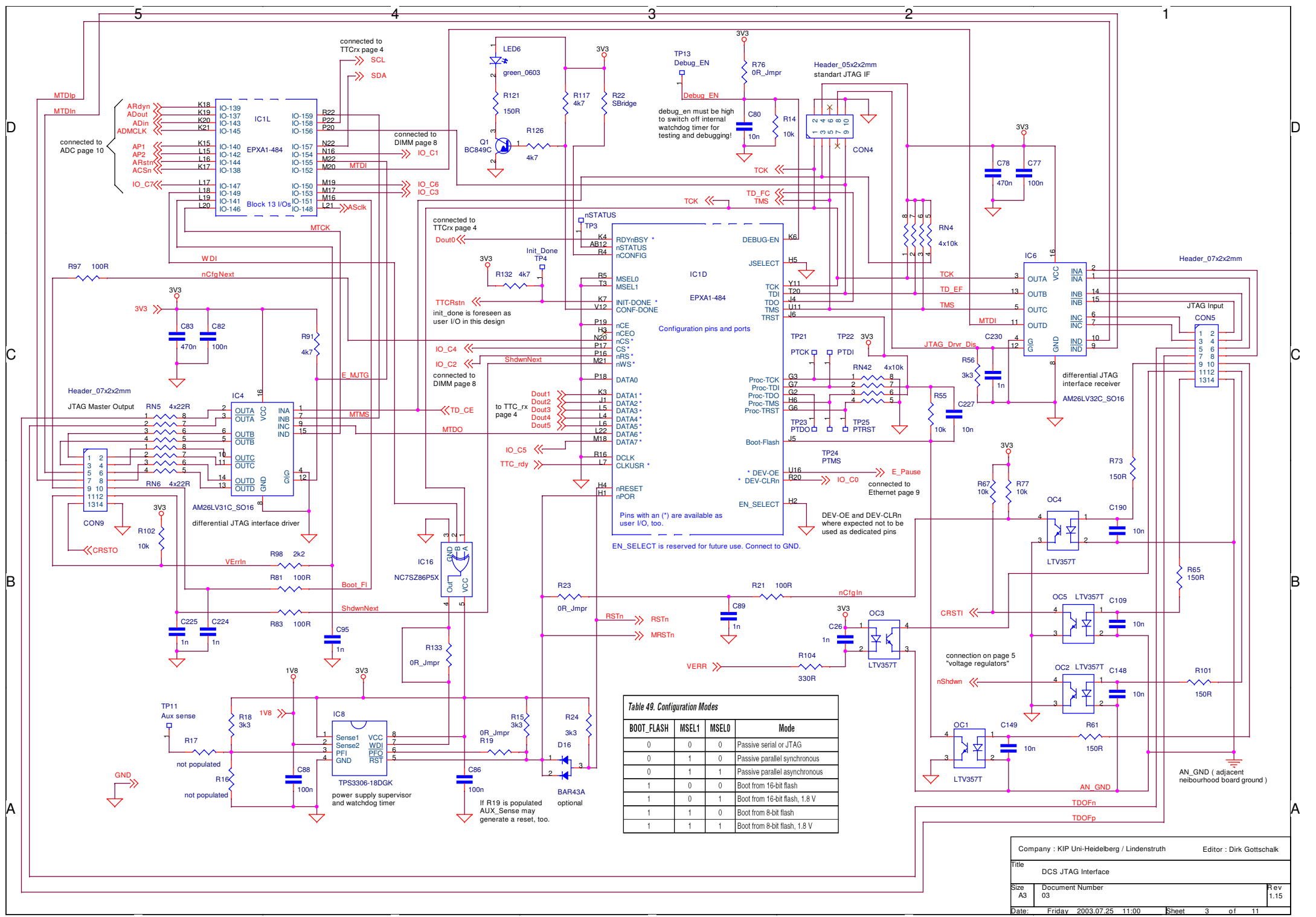
Further radiation test are in progress



Company : KIP Uni-Heidelberg / Lindenstruth		Editor : Dirk Gottschalk	
Title Overview for the DCS board			
Size A4	Document Number 01		Rev 1.16
Date: Tuesday	2003.06.24	9:50	Sheet 1 of 11

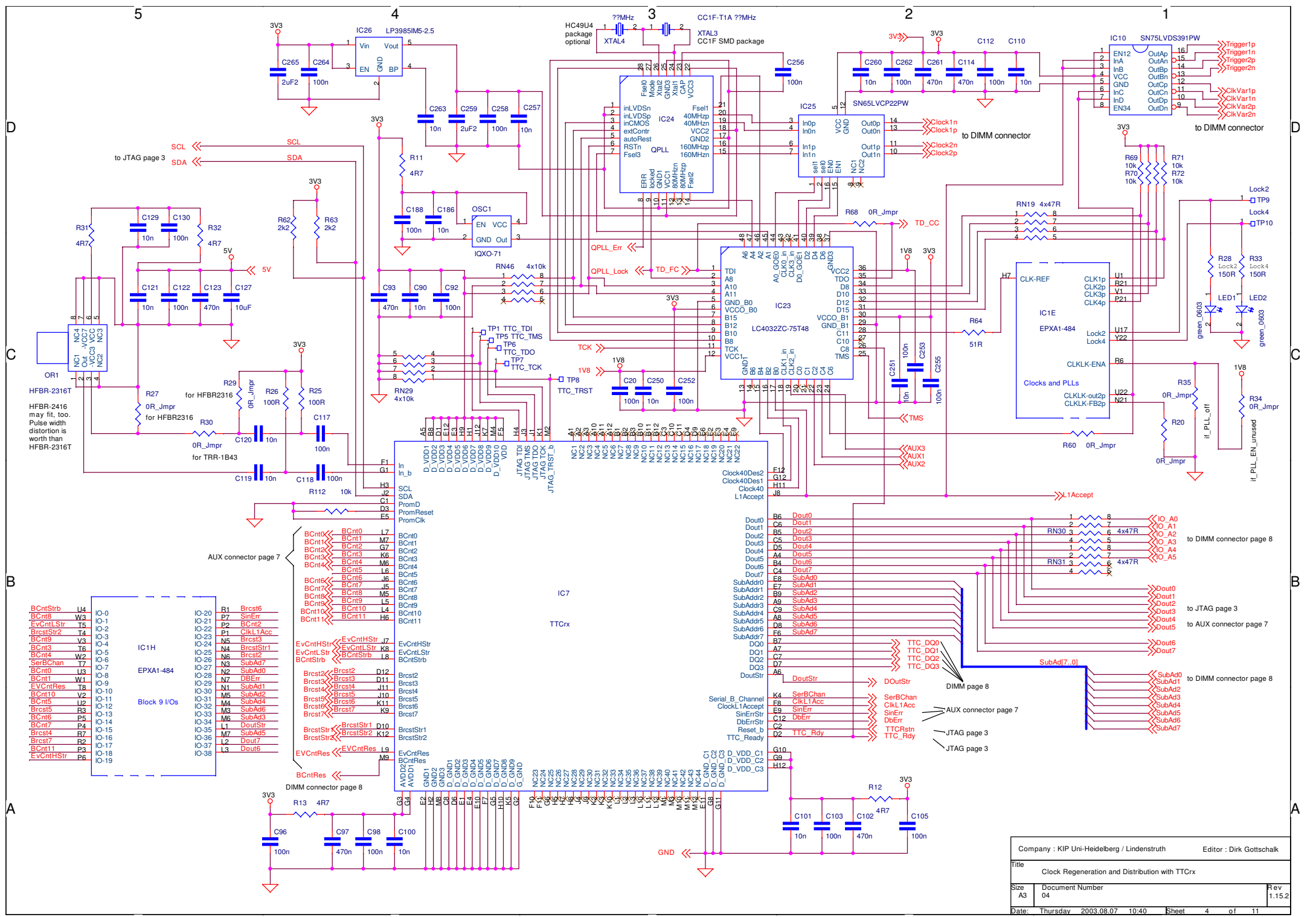


Company : KIP Uni-Heidelberg / Lindenstruth		Editor : Dirk Gottschalk	
Title DCS SDRAM Interface			
Size A3	Document Number 02		Rev 1.15
Date: Tuesday 2003.07.22 15:00	Sheet 2	of 11	



**Table 49. Configuration Modes**

BOOT_FLASH	MSEL1	MSEL0	Mode
0	0	0	Passive serial or JTAG
0	1	0	Passive parallel synchronous
0	1	1	Passive parallel asynchronous
1	0	0	Boot from 16-bit flash
1	0	1	Boot from 16-bit flash, 1.8 V
1	1	0	Boot from 8-bit flash
1	1	1	Boot from 8-bit flash, 1.8 V



IC1H  
EPXA1-484  
Block 9 I/Os

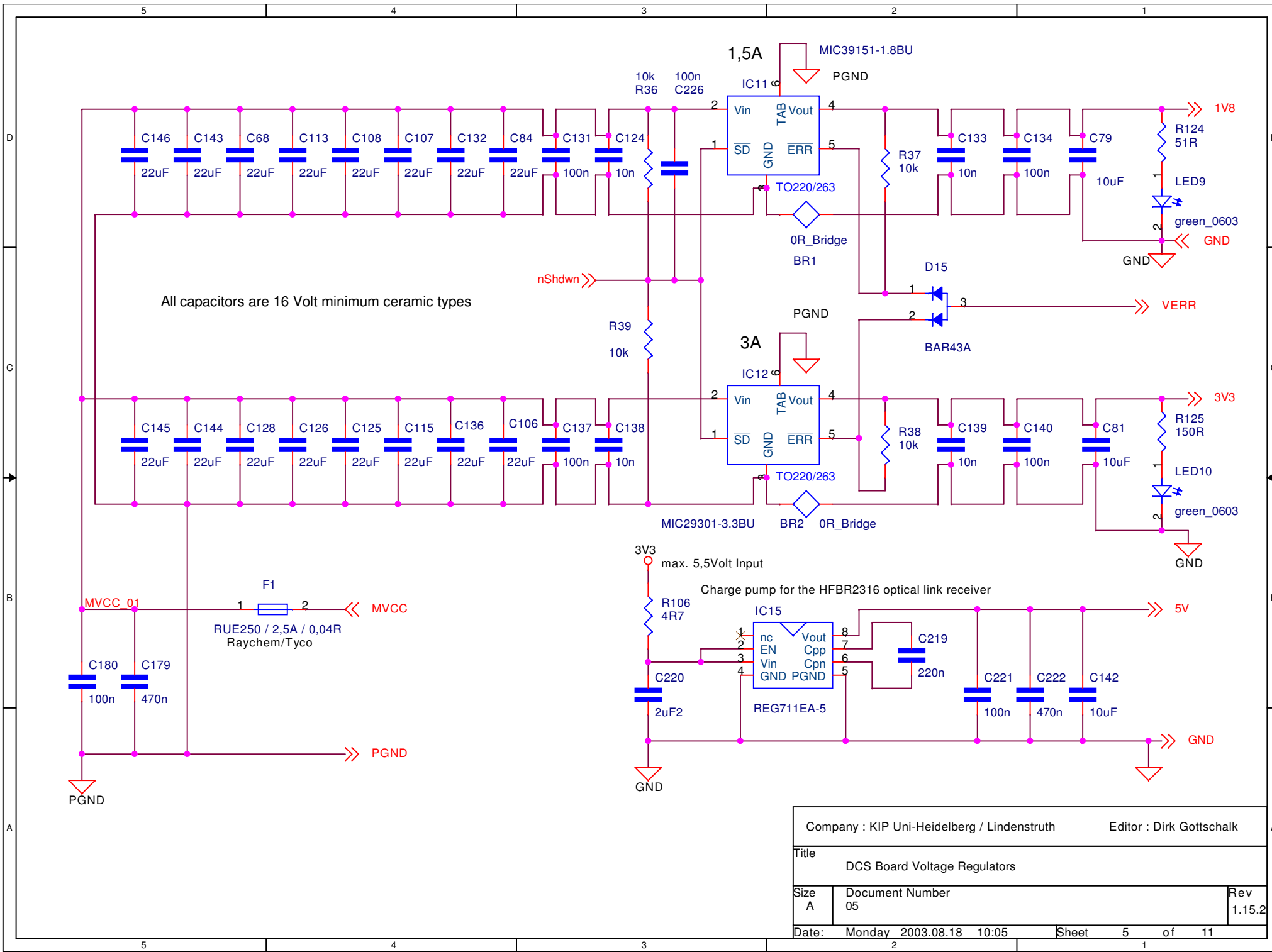
BCntStrb	U4	IO-0	R1	Brcst6	IO-20
BCnt6	W3	IO-1	P7	SinErr	IO-21
EvCntLStr	T5	IO-2	P2	BCnt2	IO-22
BrcstStr2	T4	IO-3	P1	ClkL1Acc	IO-23
BCnt9	V3	IO-4	N5	Brcst3	IO-24
BCnt3	T6	IO-5	N4	BrcstStr1	IO-25
BCnt4	W2	IO-6	N6	Brcst2	IO-26
SerBChan	U3	IO-7	N2	SubAd7	IO-27
BCnt0	L3	IO-8	N7	DBErr	IO-28
BCnt1	W1	IO-9	N1	SubAd1	IO-29
EVCntRes	T8	IO-10	N3	SubAd2	IO-30
BCnt10	V2	IO-11	M5	SubAd2	IO-31
BCnt5	U2	IO-12	M4	SubAd4	IO-32
Brcst5	B3	IO-13	M3	SubAd6	IO-33
BCnt6	P5	IO-14	M6	SubAd3	IO-34
BCnt7	P4	IO-15	L1	DoutStr	IO-35
Brcst4	R7	IO-16	M7	SubAd5	IO-36
Brcst7	P2	IO-17	L2	Dout7	IO-37
BCnt11	P3	IO-18	L3	Dout6	IO-38
EvCntHStr	P6	IO-19	M9	EvCntRes	IO-39

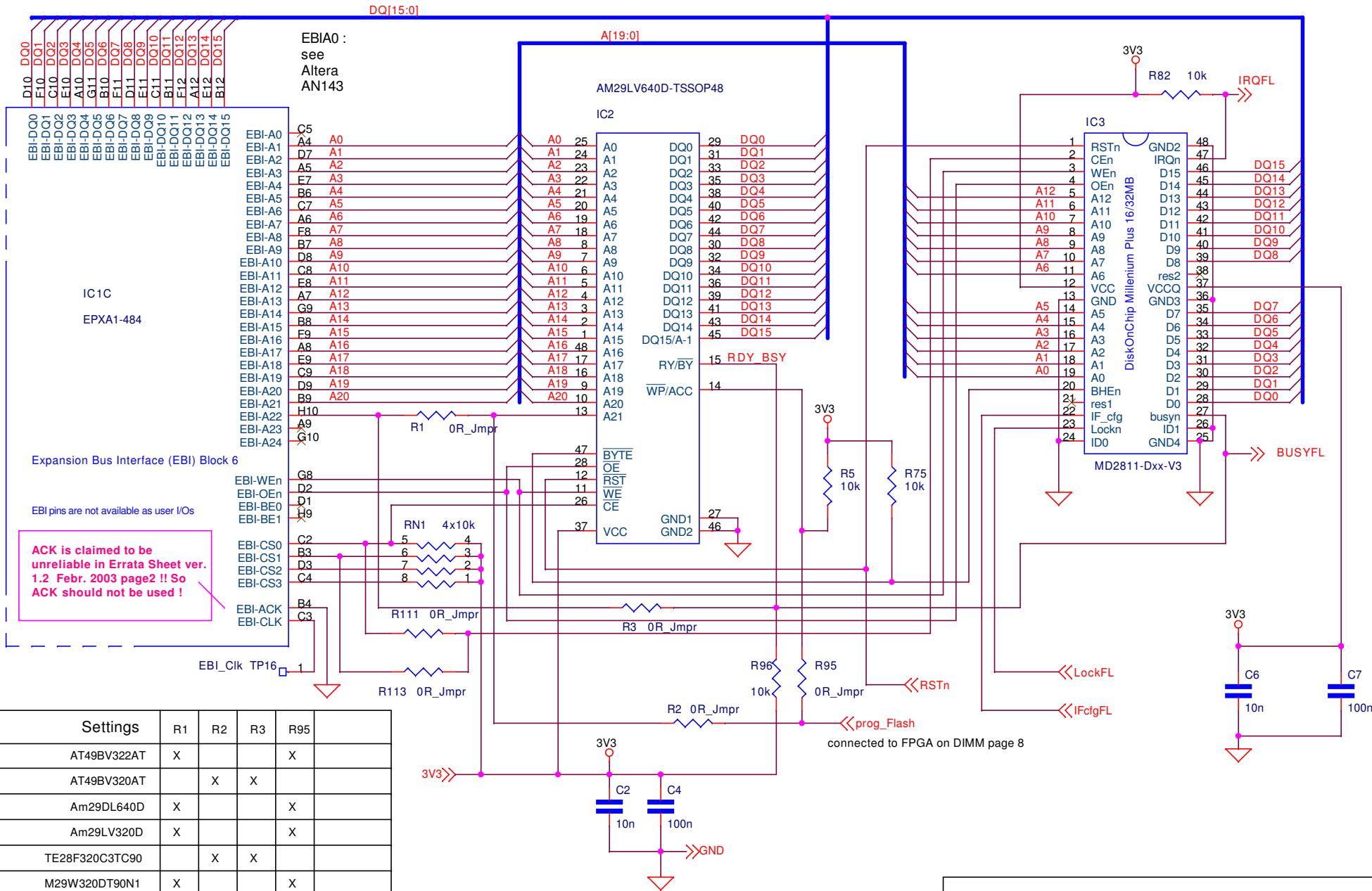
AUX connector page 7

BCnt0	BCnt0	L7	BCnt0
BCnt1	BCnt1	M7	BCnt1
BCnt2	BCnt2	G7	BCnt2
BCnt3	BCnt3	K6	BCnt3
BCnt4	BCnt4	M6	BCnt4
BCnt5	BCnt5	L6	BCnt5
BCnt6	BCnt6	J6	BCnt6
BCnt7	BCnt7	J5	BCnt7
BCnt8	BCnt8	M8	BCnt8
BCnt9	BCnt9	L5	BCnt9
BCnt10	BCnt10	L4	BCnt10
BCnt11	BCnt11	H6	BCnt11

IC7  
TTCrx

EvCntHStr	EvCntHStr	J7	EvCntHStr
EvCntLStr	EvCntLStr	K8	EvCntLStr
BCntStrb	BCntStrb	L8	BCntStrb
Brcst2	Brcst2	D12	Brcst2
Brcst3	Brcst3	D11	Brcst3
Brcst4	Brcst4	J11	Brcst4
Brcst5	Brcst5	J10	Brcst5
Brcst6	Brcst6	K11	Brcst6
Brcst7	Brcst7	K9	Brcst7
BrcstStr1	BrcstStr1	D10	BrcstStr1
BrcstStr2	BrcstStr2	K12	BrcstStr2
EVCntRes	EVCntRes	L9	EVCntRes
BCntRes	BCntRes	M9	BCntRes





Expansion Bus Interface (EBI) Block 6

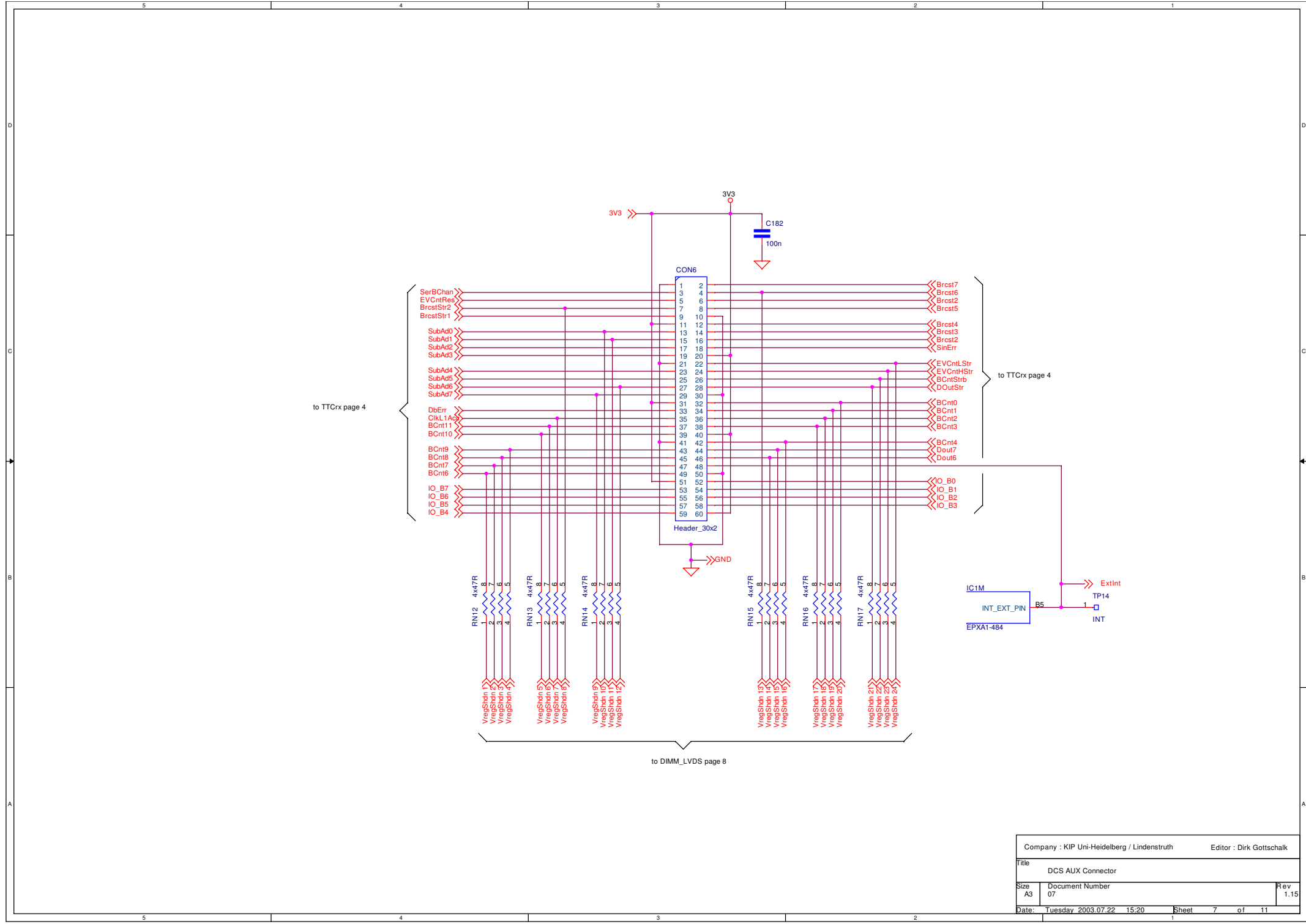
EBI pins are not available as user I/Os

ACK is claimed to be unreliable in Errata Sheet ver. 1.2 Febr. 2003 page2 !! So ACK should not be used !

Settings	R1	R2	R3	R95
AT49BV322AT	X			X
AT49BV320AT		X	X	
Am29DL640D	X			X
Am29LV320D	X			X
TE28F320C3TC90		X	X	
M29W320DT90N1	X			X
MBM29DL164TD	X			X
MBM29DL32xTE	X			X

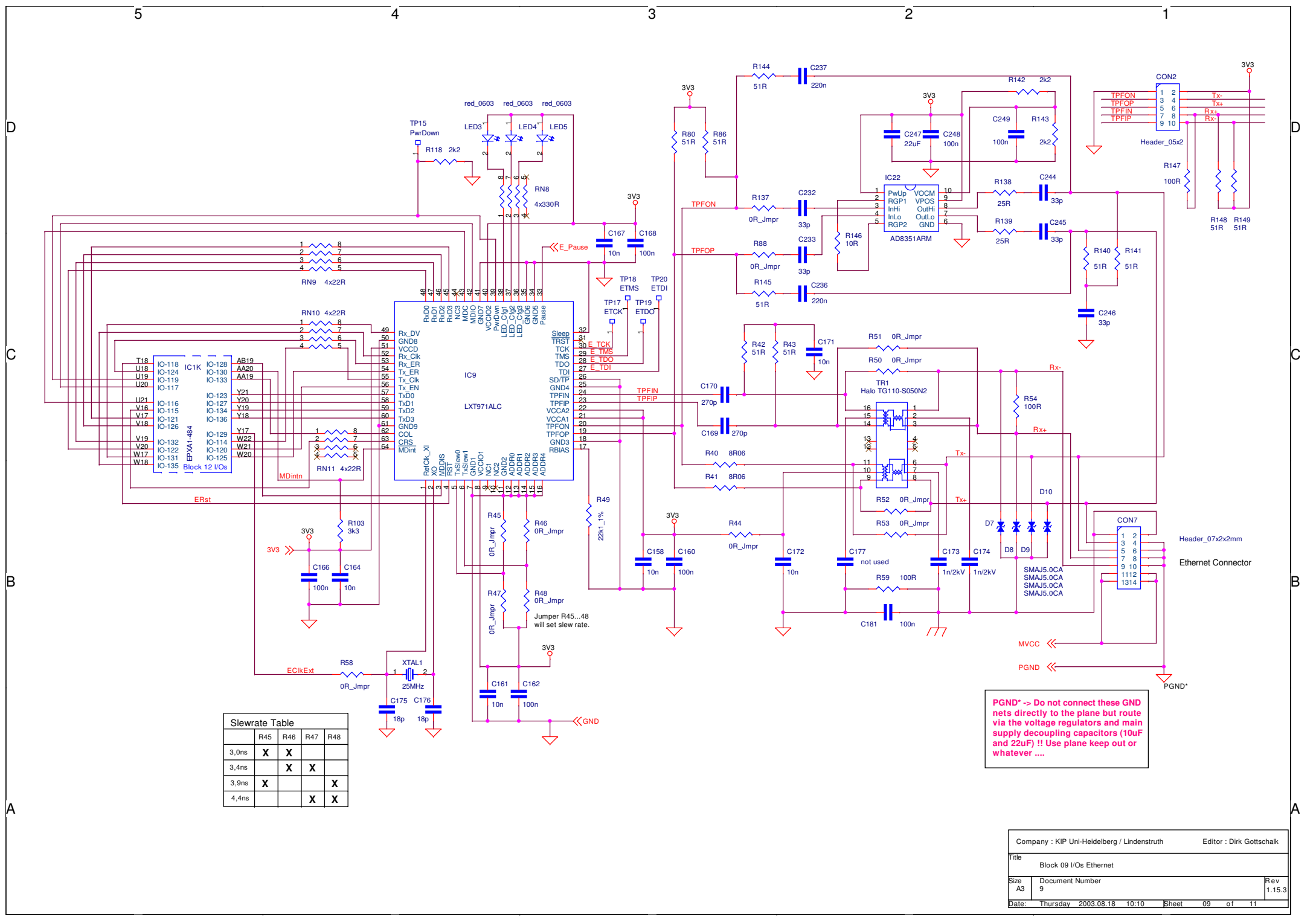
There are two types of Flash Eproms. Pins 9, 13, 14 and 15 are connected disparately. Especially address pins 19 and 21 are exchanged.

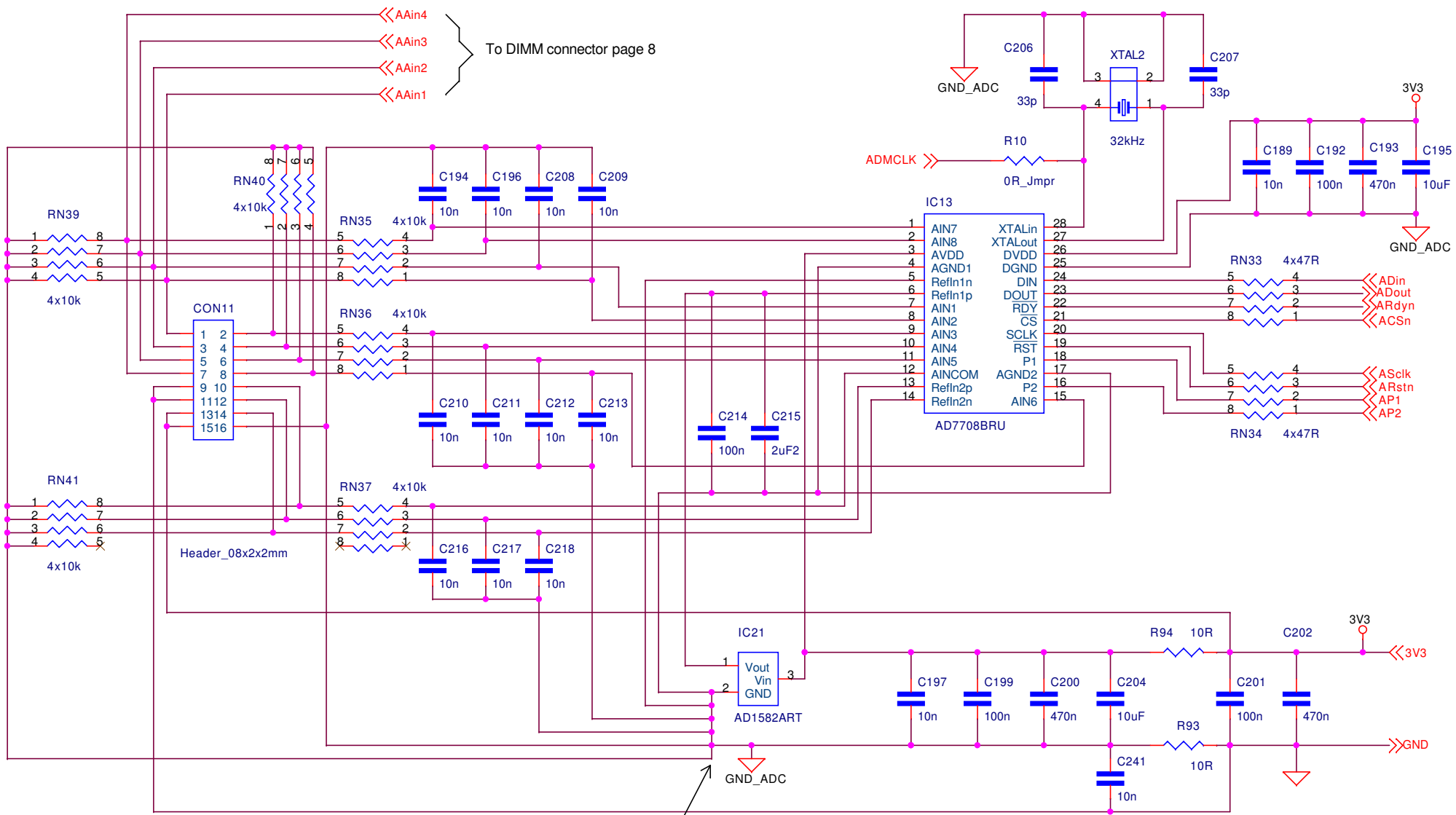
Company : KIP Uni-Heidelberg / Lindenstruth		Editor : Dirk Gottschalk	
Title Expansion Bus Interface (EBI)			
Size A4	Document Number 06	Rev 1.15	
Date:	Tuesday 2003.07.22 15:15	Sheet	6 of 11



Company : KIP Uni-Heidelberg / Lindenstruth		Editor : Dirk Gottschalk	
Title DCS AUX Connector			
Size A3	Document Number 07	Rev 1.15	
Date: Tuesday 2003.07.22 15:20	Sheet 7	of 11	



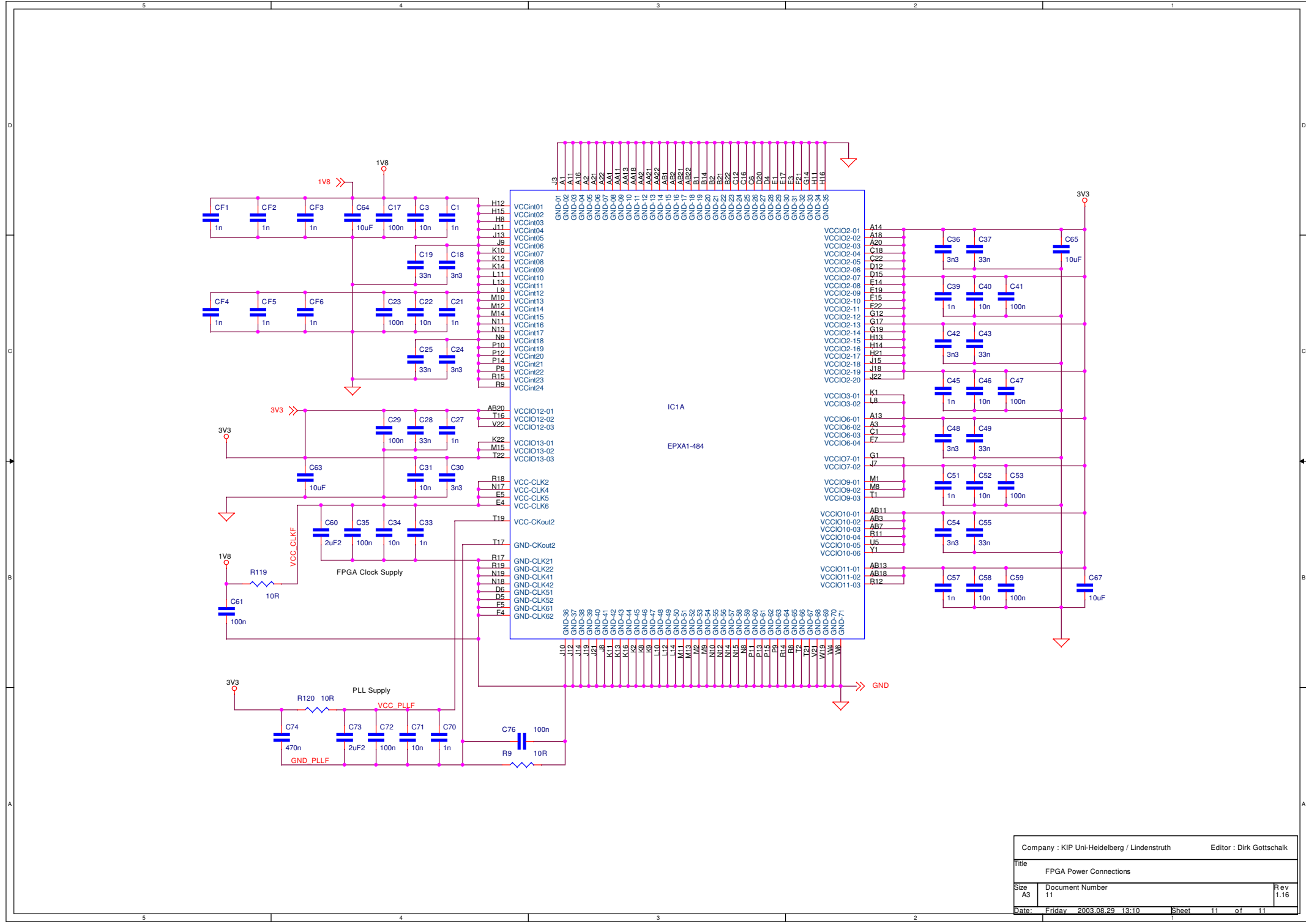




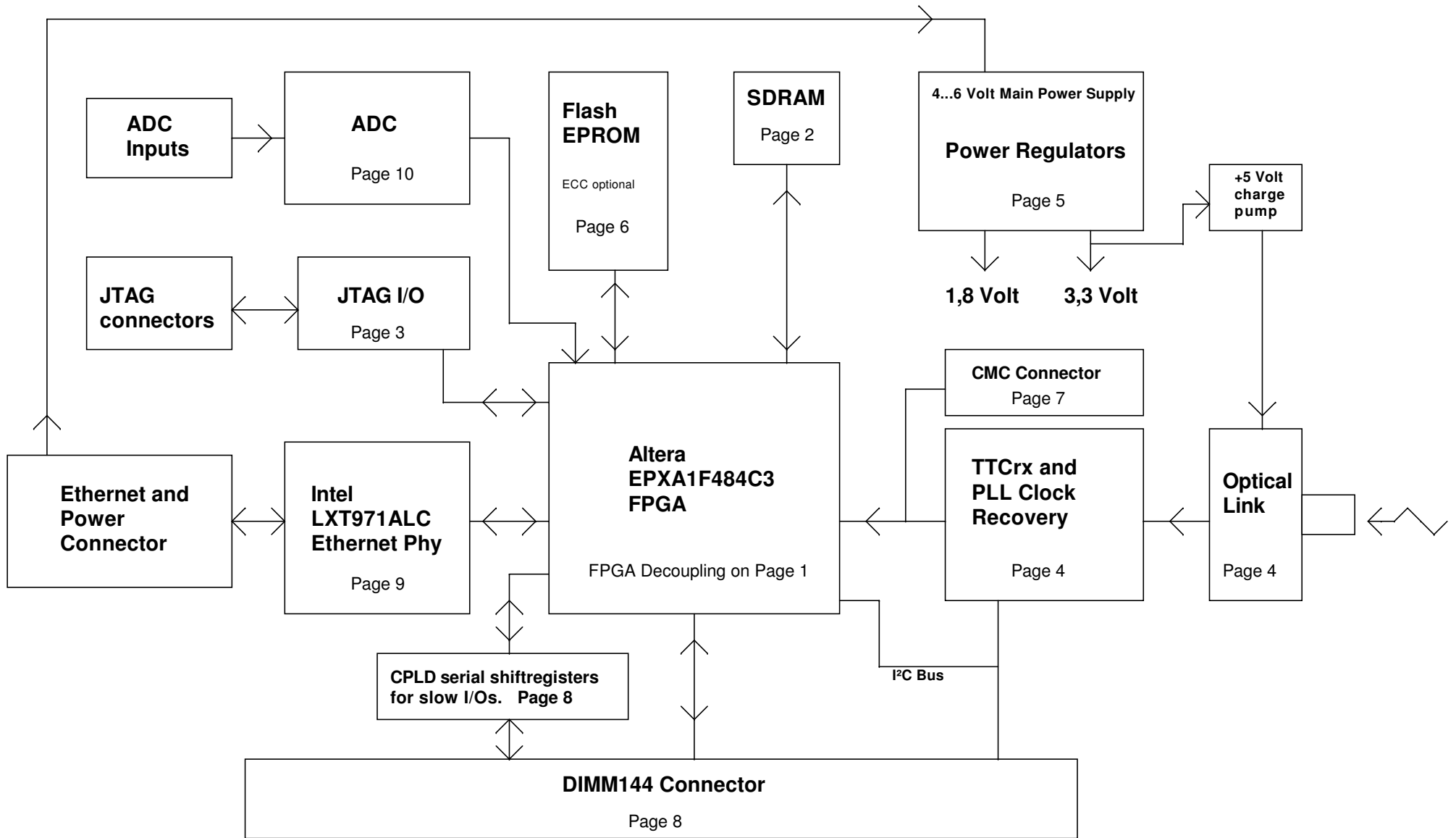
To DIMM connector page 8

Please connect these analog ground lines to one point near voltage reference !

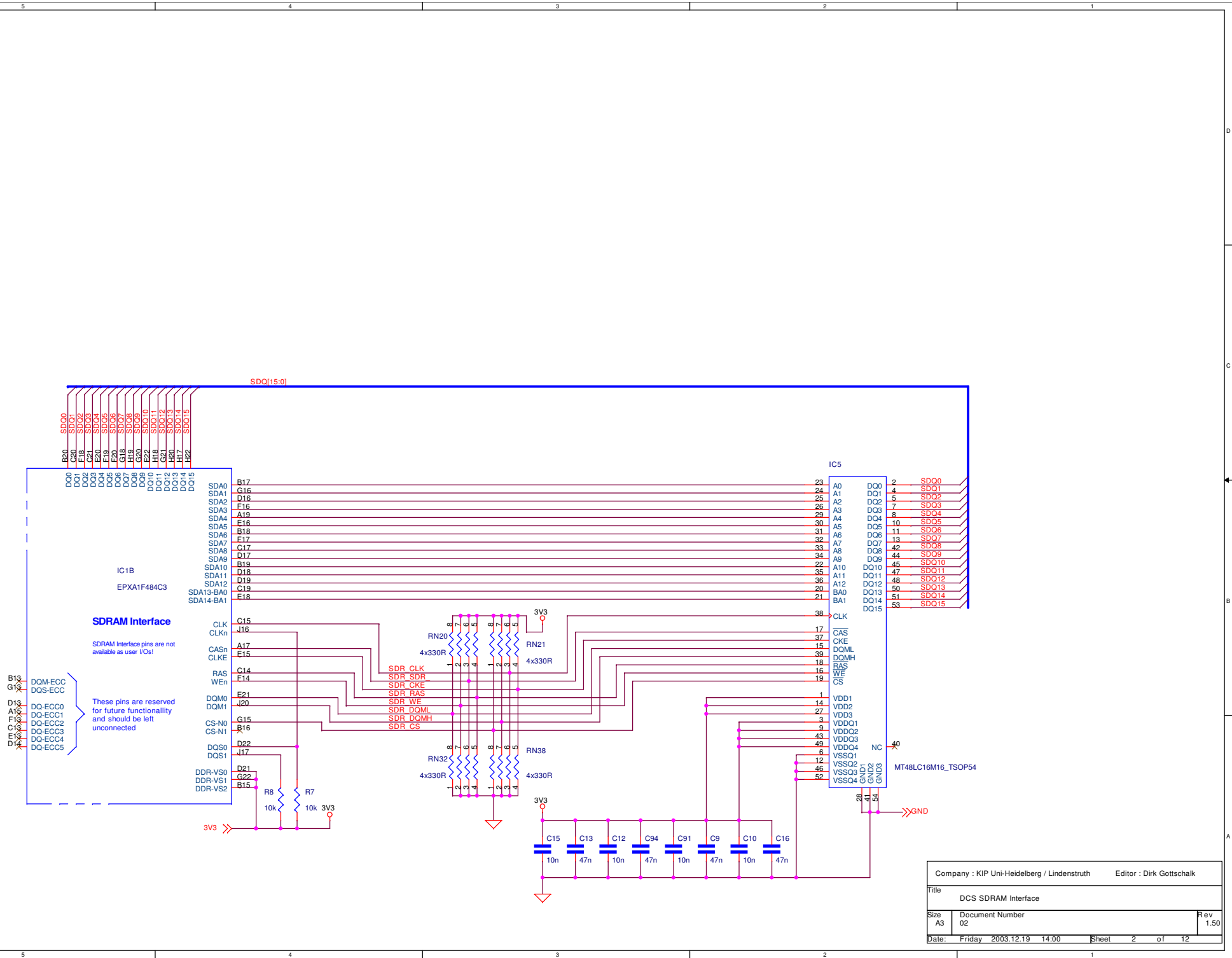
Company : KIP Uni-Heidelberg / Lindenstruth		Editor : Dirk Gottschalk	
Title DCS ADC			
Size A4	Document Number 10		Rev 1.15
Date: Monday 2003.07.22 16:00	Sheet 10	of 11	



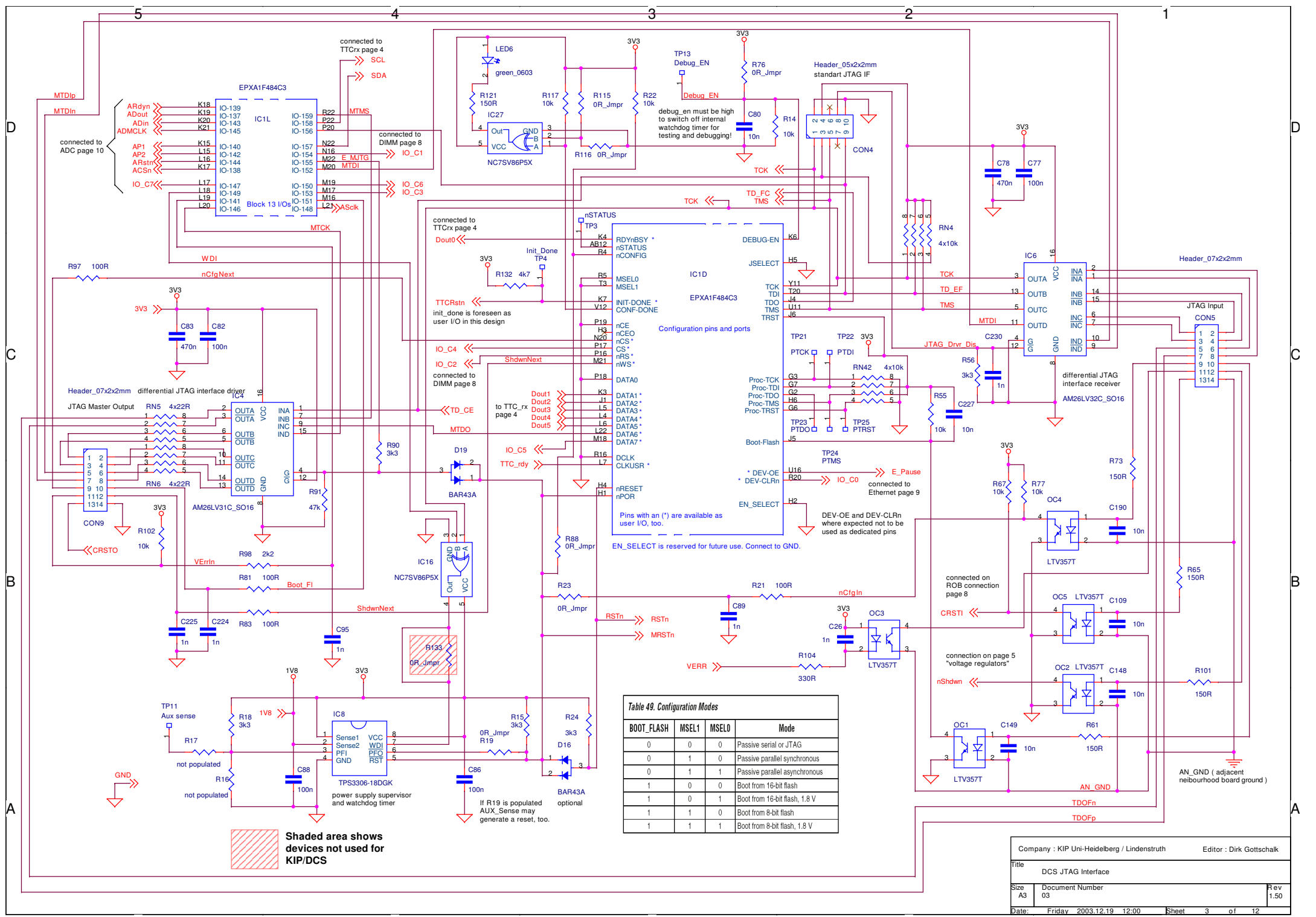
Company : KIP Uni-Heidelberg / Lindenstruth		Editor : Dirk Gottschalk	
Title FPGA Power Connections			
Size A3	Document Number 11	Rev 1.16	
Date: Friday 2003.08.29 13:10	Sheet 11	of 11	



Company : KIP Uni-Heidelberg / Lindenstruth		Editor : Dirk Gottschalk	
Title Overview for the DCS board			
Size A4	Document Number 01		Rev 1.51
Date: Monday	2004.01.27	14:15	Sheet 1 of 12



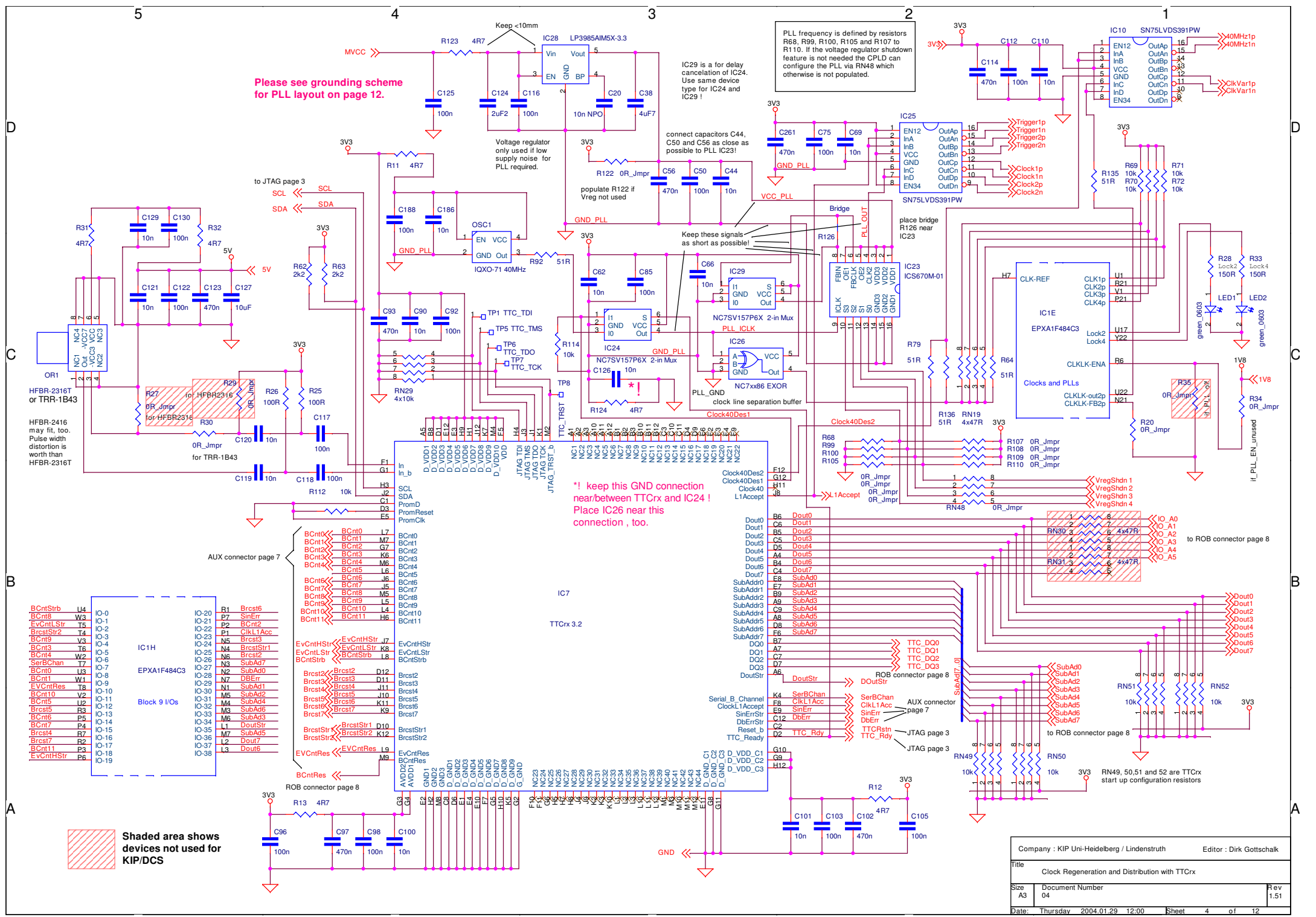
Company : KIP Uni-Heidelberg / Lindenstruth		Editor : Dirk Gottschalk	
Title DCS SDRAM Interface			
Size A3	Document Number 02		Rev 1.50
Date: Friday, 2003.12.19 14:00	Sheet 2	of 12	



**Table 49. Configuration Modes**

BOOT_FLASH	MSEL1	MSEL0	Mode
0	0	0	Passive serial or JTAG
0	1	0	Passive parallel synchronous
0	1	1	Passive parallel asynchronous
1	0	0	Boot from 16-bit flash
1	0	1	Boot from 16-bit flash, 1.8 V
1	1	0	Boot from 8-bit flash
1	1	1	Boot from 8-bit flash, 1.8 V

**Shaded area shows devices not used for KIP/DCS**



Please see grounding scheme for PLL layout on page 12.

PLL frequency is defined by resistors R68, R99, R100, R105 and R107 to R110. If the voltage regulator shutdown feature is not needed the CPLD can configure the PLL via RN48 which otherwise is not populated.

IC29 is a for delay cancelation of IC24. Use same device type for IC24 and IC29!

Voltage regulator only used if low supply noise for PLL required.

connect capacitors C44, C50 and C56 as close as possible to PLL IC23!

populate R122 if Vreg not used

Keep these signals as short as possible!

\*! keep this GND connection near/between TTCrx and IC24! Place IC26 near this connection, too.

AUX connector page 7

to ROB connector page 8

to ROB connector page 8

to ROB connector page 8

to ROB connector page 8

to ROB connector page 8

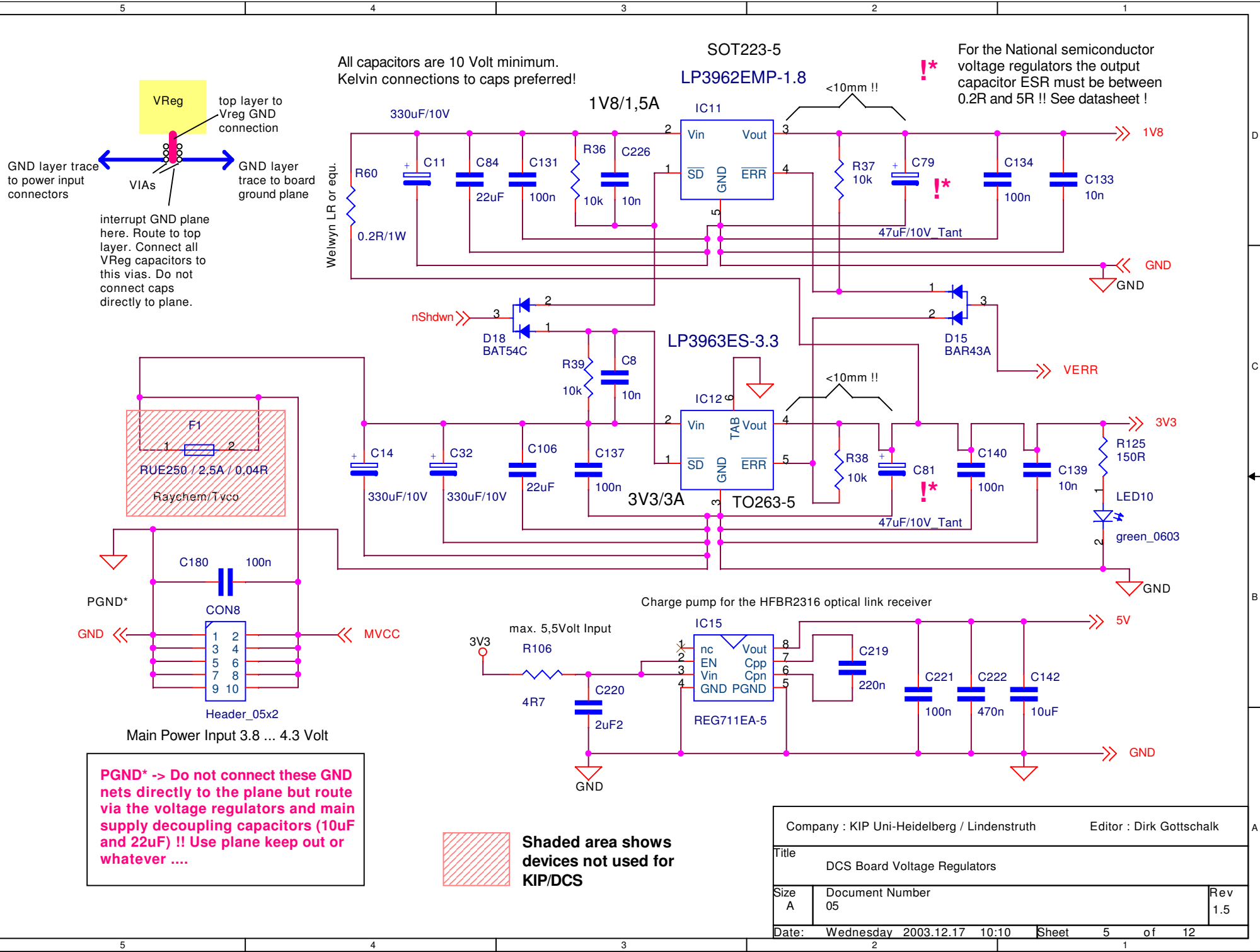
to ROB connector page 8

to ROB connector page 8

to ROB connector page 8

Shaded area shows devices not used for KIP/DCS

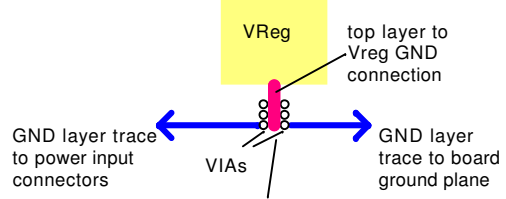
Company : KIP Uni-Heidelberg / Lindenstruth		Editor : Dirk Gottschalk
Title : Clock Regeneration and Distribution with TTCrx		
Size : A3	Document Number : 04	Rev : 1.51
Date : Thursday, 2004.01.29 12:00	Sheet : 4	of 12



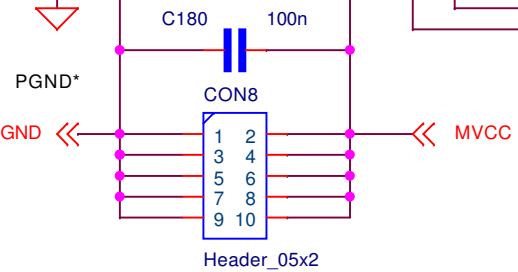
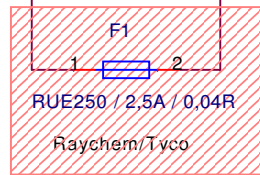
All capacitors are 10 Volt minimum.  
Kelvin connections to caps preferred!

SOT223-5  
LP3962EMP-1.8

For the National semiconductor voltage regulators the output capacitor ESR must be between 0.2R and 5R !! See datasheet !



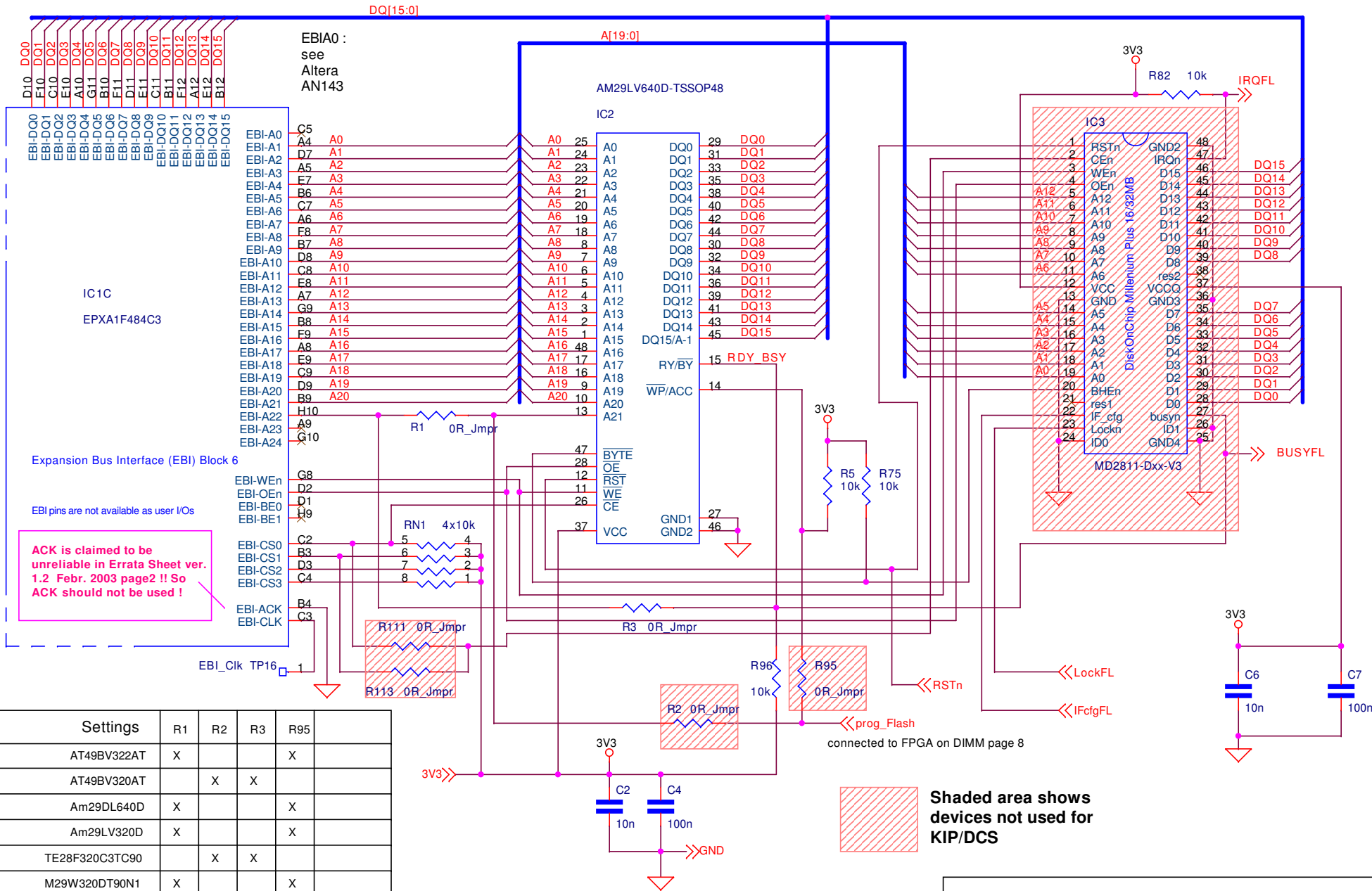
interrupt GND plane here. Route to top layer. Connect all VReg capacitors to this vias. Do not connect caps directly to plane.



**PGND\* -> Do not connect these GND nets directly to the plane but route via the voltage regulators and main supply decoupling capacitors (10uF and 22uF) !! Use plane keep out or whatever ....**

**Shaded area shows devices not used for KIP/DCS**

Company : KIP Uni-Heidelberg / Lindenstruth		Editor : Dirk Gottschalk	
Title DCS Board Voltage Regulators			
Size A	Document Number 05		Rev 1.5
Date:	Wednesday 2003.12.17 10:10	Sheet	5 of 12



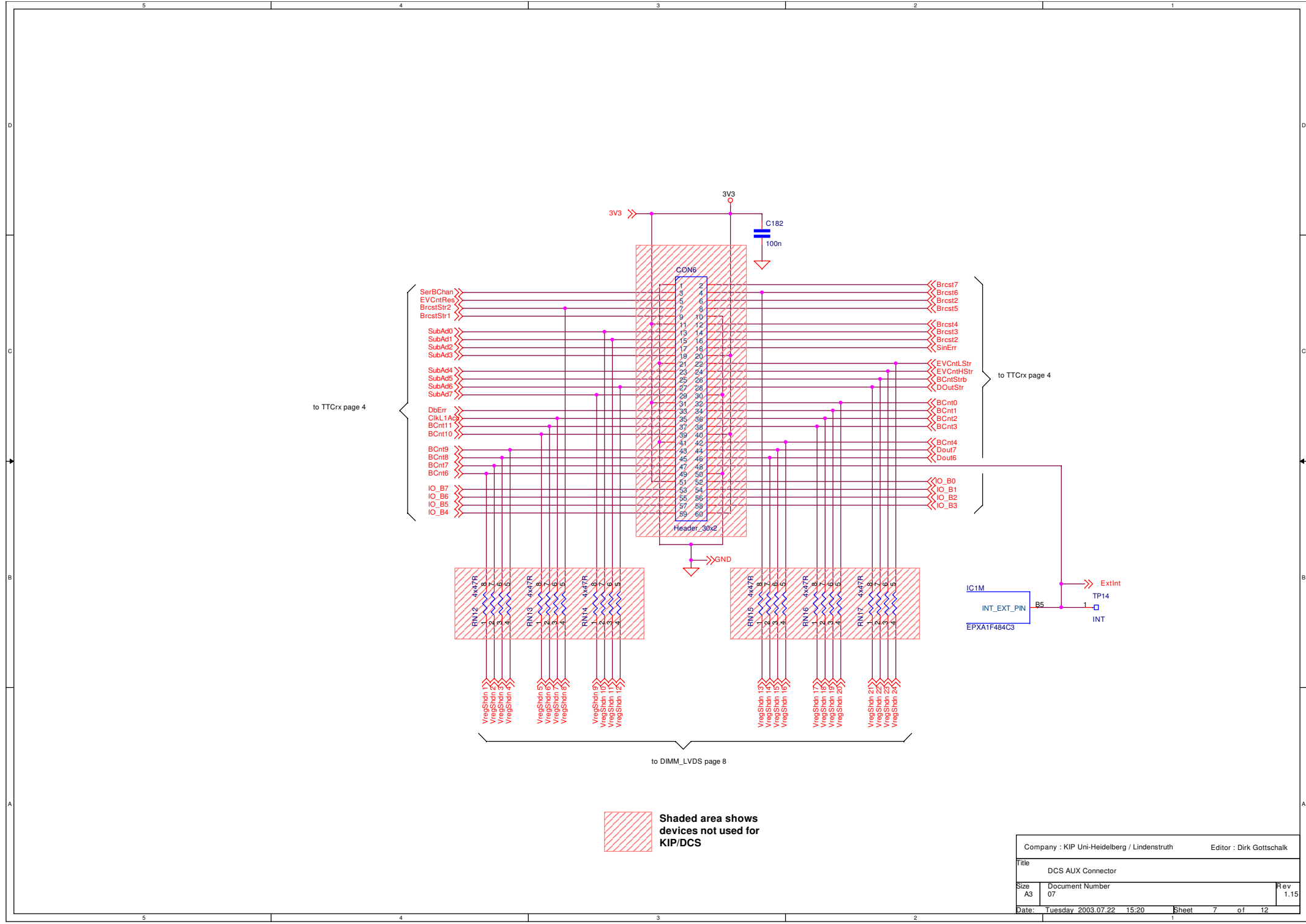
ACK is claimed to be unreliable in Errata Sheet ver. 1.2 Febr. 2003 page2 !! So ACK should not be used !

Settings	R1	R2	R3	R95
AT49BV322AT	X			X
AT49BV320AT		X	X	
Am29DL640D	X			X
Am29LV320D	X			X
TE28F320C3TC90		X	X	
M29W320DT90N1	X			X
MBM29DL164TD	X			X
MBM29DL32xTE	X			X

There are two types of Flash Eproms. Pins 9, 13, 14 and 15 are connected disparately. Especially address pins 19 and 21 are exchanged.

Shaded area shows devices not used for KIP/DCS


Company : KIP Uni-Heidelberg / Lindenstruth		Editor : Dirk Gottschalk	
Title Expansion Bus Interface (EBI)			
Size A4	Document Number 06		Rev 1.15
Date:	Tuesday	2003.07.22 15:15	Sheet 6 of 12



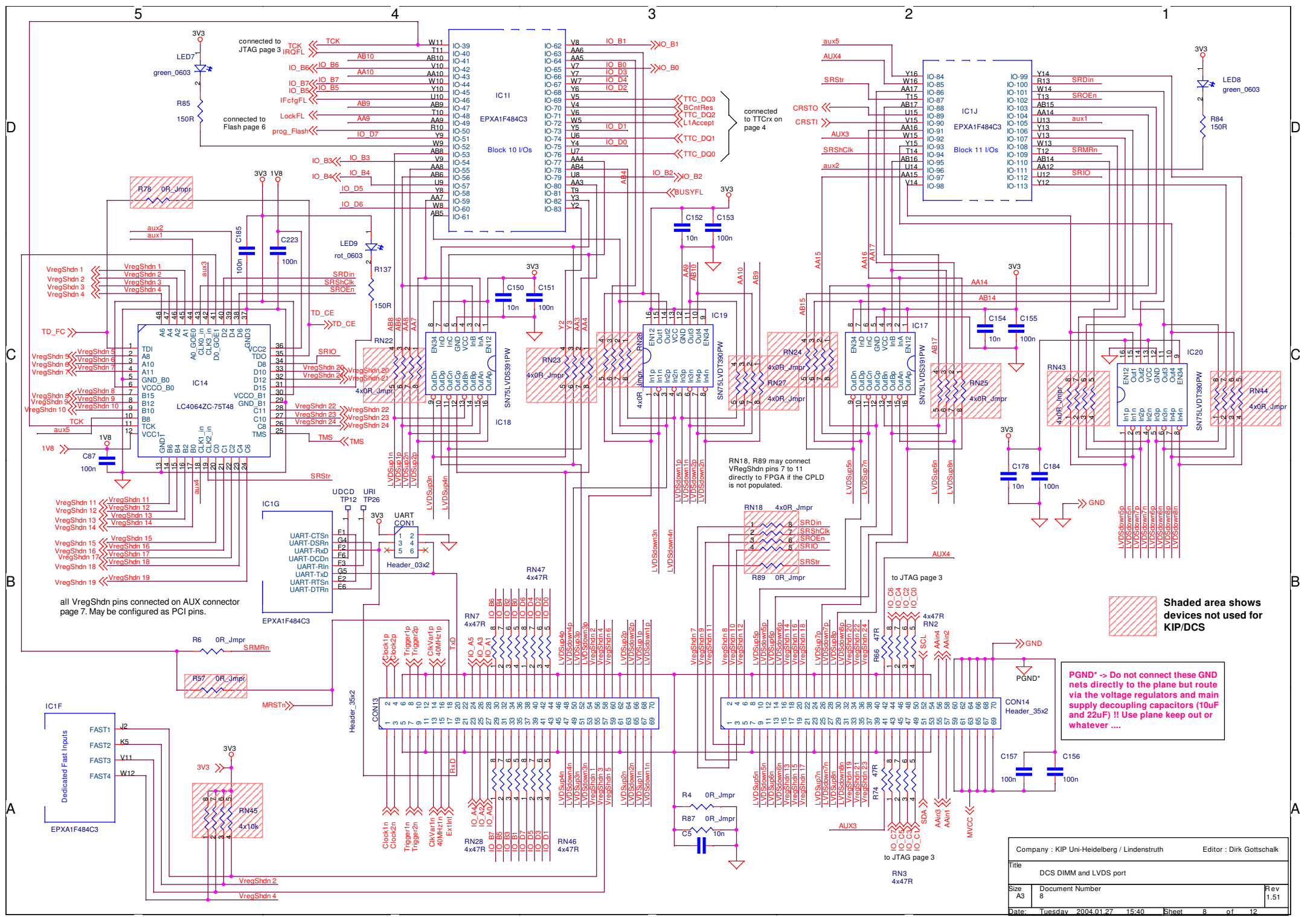
to TTCrx page 4

to TTCrx page 4

to DIMM\_LVDS page 8

 Shaded area shows devices not used for KIP/DCS

Company : KIP Uni-Heidelberg / Lindenstruth		Editor : Dirk Gottschalk	
Title DCS AUX Connector			
Size A3	Document Number 07	Rev 1.15	
Date: Tuesday 2003.07.22 15:20	Sheet 7	of 12	

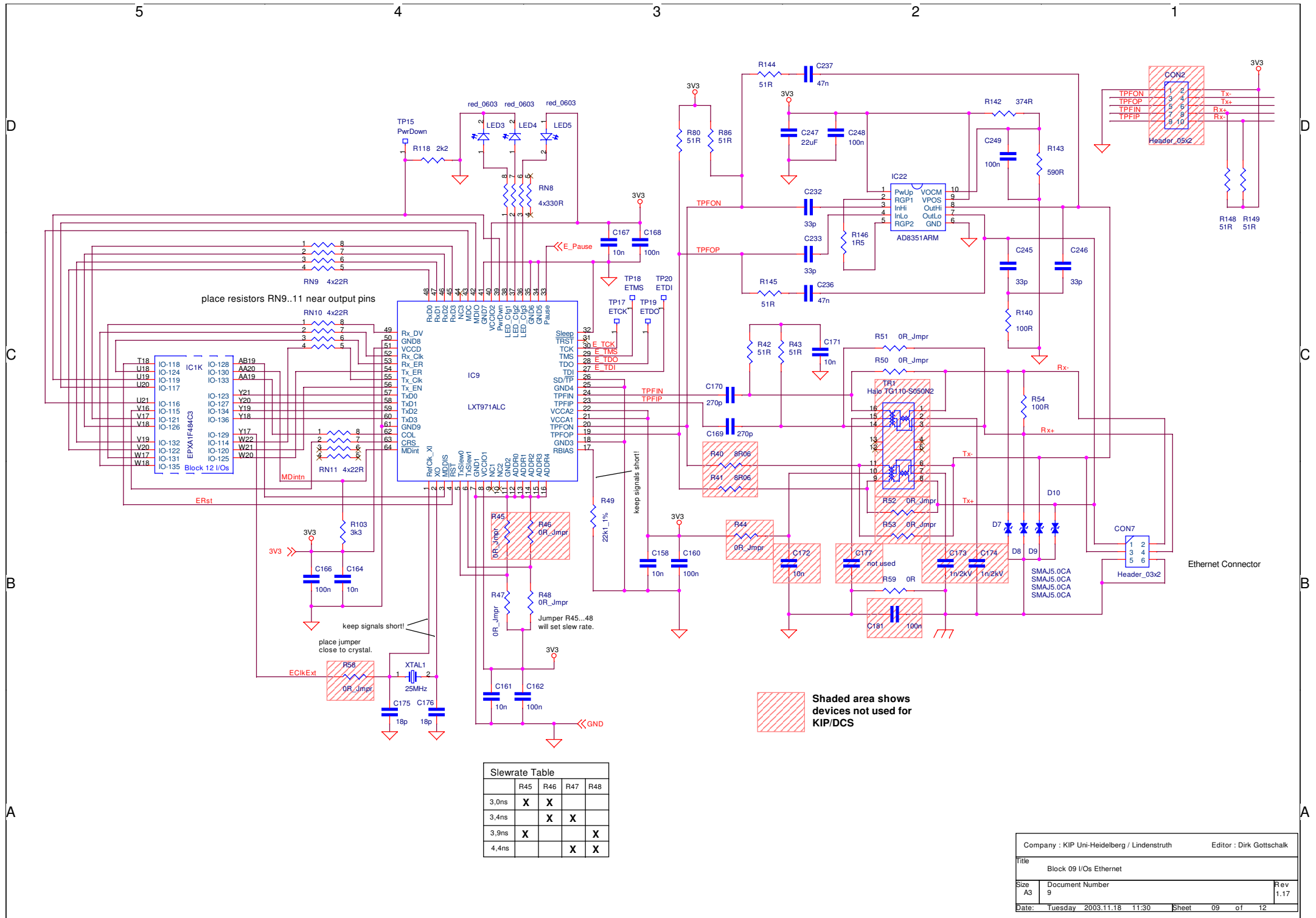


all VregShdn pins connected on AUX connector page 7. May be configured as PCI pins.

Shaded area shows devices not used for KIP/DCS

PGND\* -> Do not connect these GND nets directly to the plane but route via the voltage regulators and main supply decoupling capacitors (10uF and 22uF) !! Use plane keep out or whatever ...

Company : KIP Uni-Heidelberg / Lindenstruth		Editor : Dirk Gottschalk	
Title DCS DIMM and LVDS port			
Size A3	Document Number 8	Rev 1.51	
Date: Tuesday, 2004.01.27 15:40	Sheet 8	of 12	



place resistors RN9..11 near output pins

keep signals short!  
place jumper close to crystal.

Shaded area shows devices not used for KIP/DCS

	R45	R46	R47	R48
3,0ns	X	X		
3,4ns		X	X	
3,9ns	X			X
4,4ns			X	X

shield signals AAin1 .. 4 with GND traces

To ROB connector page 8

keep all analog signals as short as possible

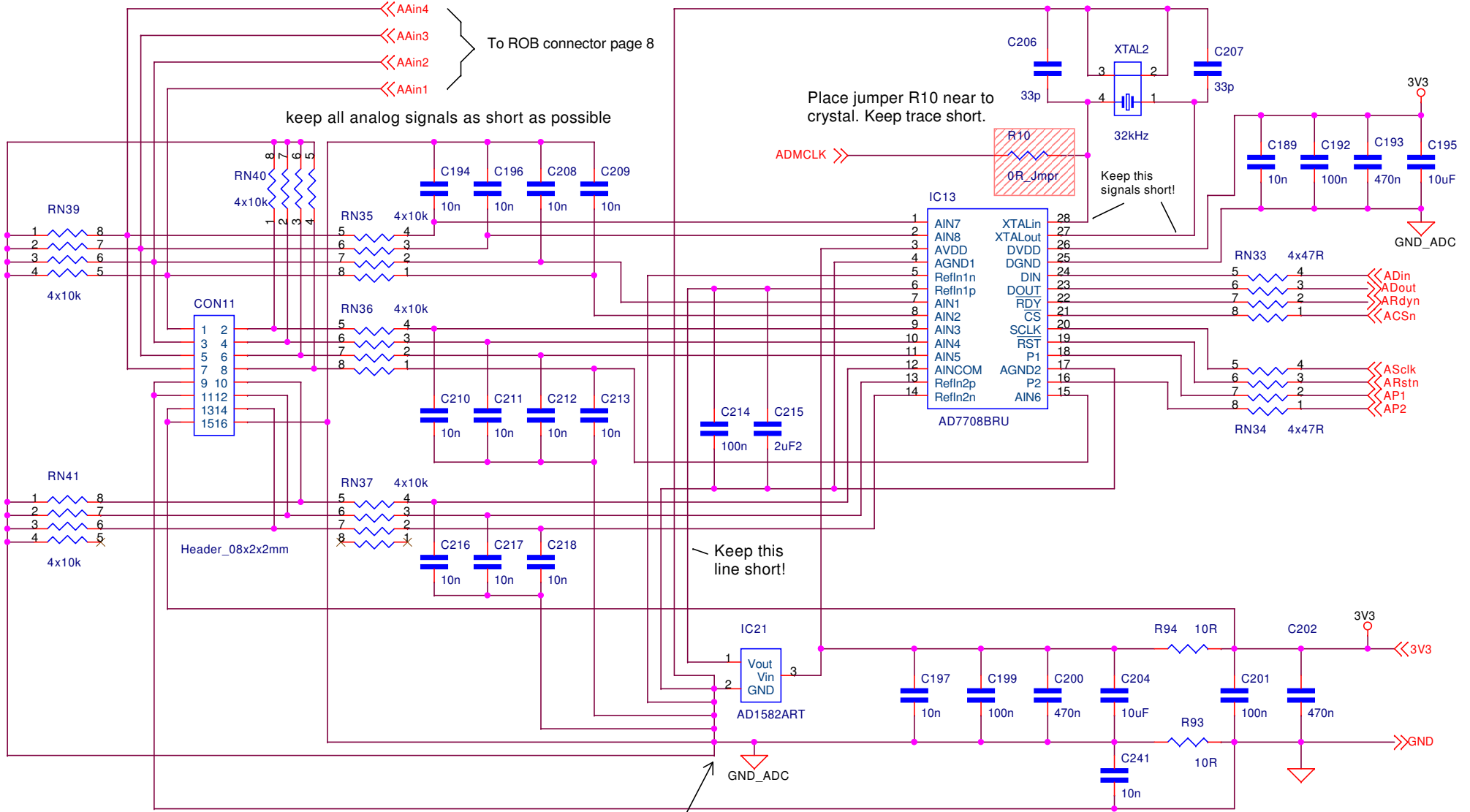
Place jumper R10 near to crystal. Keep trace short.

Keep this signals short!

Keep this line short!

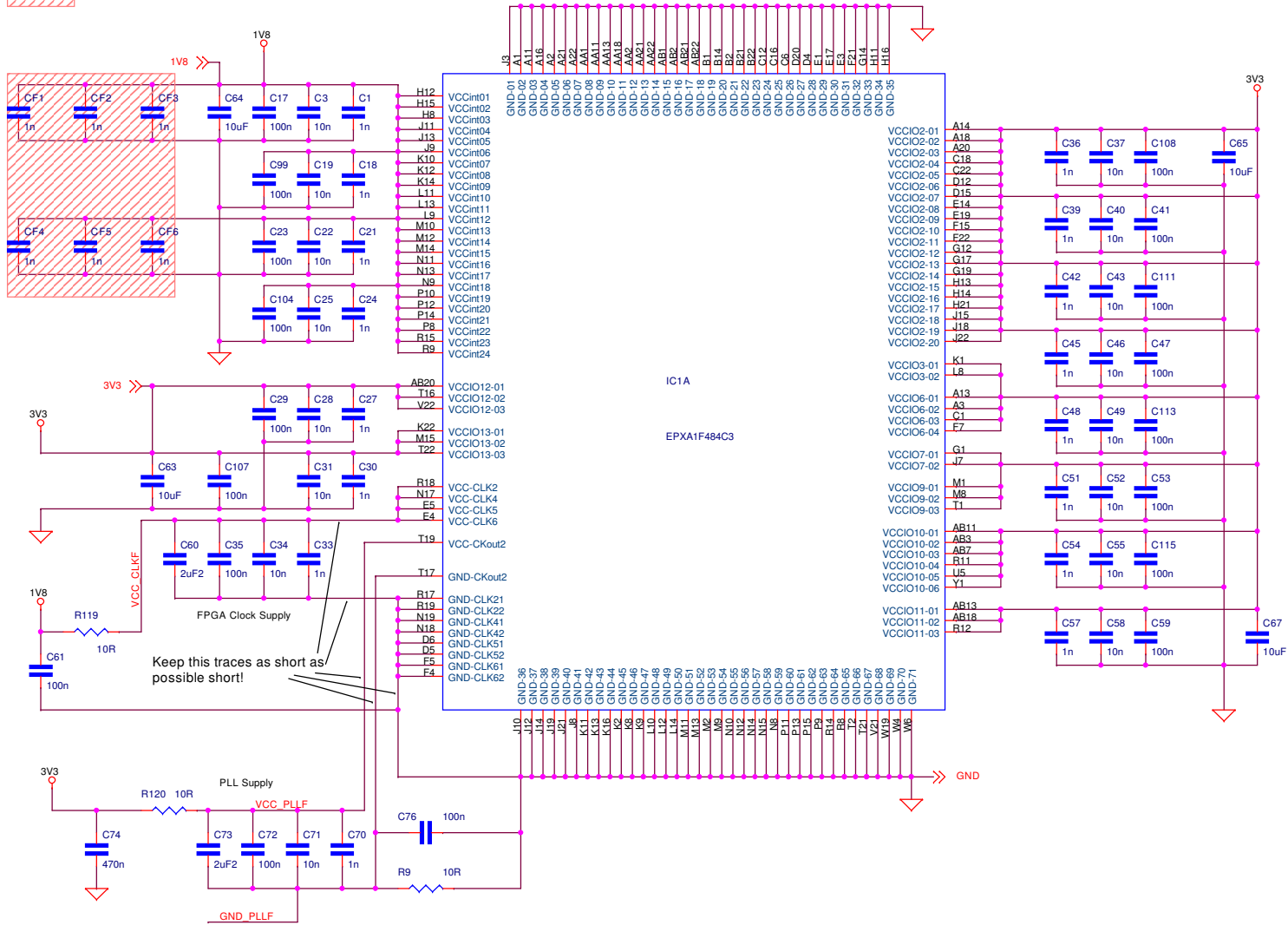
Please connect these analog ground to one point near voltage reference ! Do only connect to GND plane here with multiple vias!

 Shaded area shows devices not used for KIP/DCS



Company : KIP Uni-Heidelberg / Lindenstruth		Editor : Dirk Gottschalk
Title DCS ADC		
Size A4	Document Number 10	Rev 1.15
Date: Monday 2003.07.22 16:00	Sheet 10	of 12

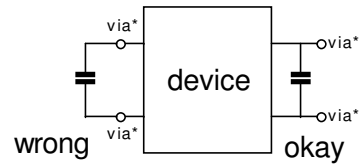
Shaded area shows devices not used for KIP/DCS



Company : KIP Uni-Heidelberg / Lindenstruth		Editor : Dirk Gottschalk	
Title FPGA Power Connections			
Size A3	Document Number 11	Rev 1.50	
Date: Friday 2003.12.19 14:30	Sheet 11	of 12	

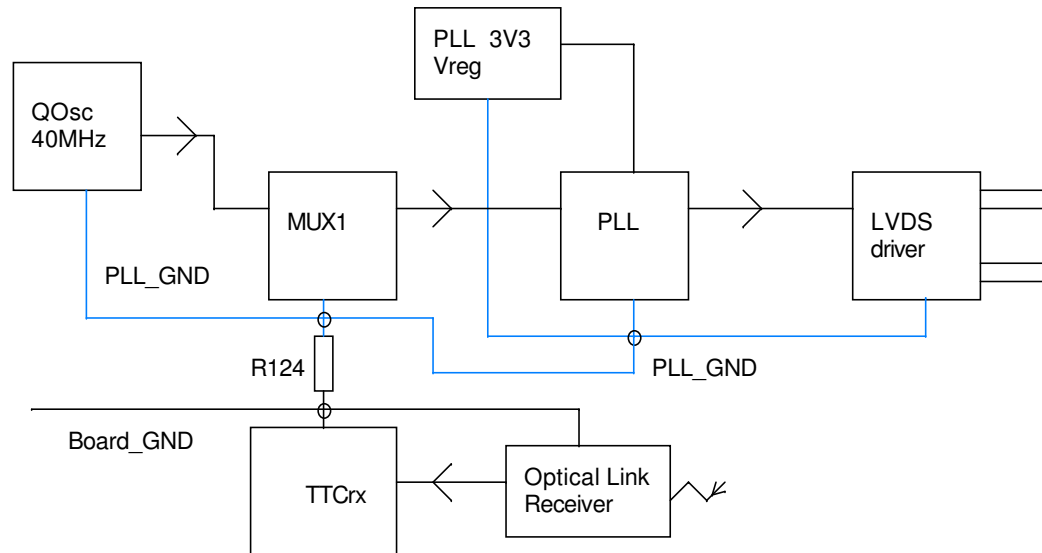
## Routing Hints for the DCS Board

Place 10nF and 100nF capacitors as close as possible to the devices. Place power vias as close as possible to the related decoupling capacitors not to the related device. This may not always work with BGAs but should work with all non BGA packages. See picture.



\*via to supply or GND planes

## Grounding scheme for PLL, TTCrx and 120MHz LVDS driver



Wednesday 2003.12.17 10:10		Editor : Dirk Gottschalk	
Title DCS Board Routing Hints			
Size A4	Document Number 12		Rev 1.19
Date: Wednesday 2003.12.17 13:30	Sheet 12	of 12	

Company : KIP Uni-Heidelberg / Lindenstruth

Bill Of Materials September 01, 2003 11:28:20 Page1

Item	Quantity	Reference	Part				
						C257,C260,C263	
	11	65	C4,C7,C15,C16,C17,C20, C23,C29,C35,C41,C47,C53, C59,C61,C72,C76,C77,C82, C86,C88,C92,C96,C98,C103, C105,C112,C117,C118,C122, C130,C131,C134,C137,C140, C151,C153,C155,C156,C157, C160,C162,C166,C168,C180, C181,C182,C184,C185,C188, C192,C199,C201,C214,C221, C223,C226,C248,C249,C252, C253,C255,C256,C258,C262, C264			100n	
1	1	CON1	Header_03x2				
2	1	CON2	Header_05x2				
3	1	CON3	DIMM144_pinrow	12	7	C18,C24,C30,C36,C42,C48, C54	3n3
4	1	CON4	Header_05x2x2mm				
5	3	CON5,CON7,CON9	Header_07x2x2mm				
6	1	CON6	Header_30x2	13	7	C19,C25,C28,C37,C43,C49, C55	33n
7	1	CON11	Header_08x2x2mm				
-----							
				14	6	C60,C73,C215,C220,C259, C265	2uF2
8	2	BR1,BR2	0R_Bridge				
9	23	CF1,C1,CF2,CF3,CF4,CF5, CF6,C9,C12,C21,C26,C27, C33,C39,C45,C51,C57,C70, C89,C95,C224,C225,C230	1n	15	10	C63,C64,C65,C67,C79,C81, C127,C142,C195,C204	10uF
				16	17	C68,C84,C106,C107,C108, C113,C115,C125,C126,C128, C132,C136,C143,C144,C145, C146,C247	22uF
10	61	C2,C3,C6,C10,C13,C22,C31, C34,C40,C46,C52,C58,C71, C80,C90,C100,C101,C109, C110,C119,C120,C121,C124, C129,C133,C138,C139,C148, C149,C150,C152,C154,C158, C161,C164,C167,C171,C172, C178,C186,C189,C190,C194, C196,C197,C208,C209,C210, C211,C212,C213,C216,C217, C218,C227,C241,C250,C251,	10n	17	14	C74,C78,C83,C93,C97,C102, C114,C123,C179,C193,C200, C202,C222,C261	470n
				18	2	C170,C169	270p
				19	2	C173,C174	1n/2kV
				20	2	C175,C176	18p

21	1	C177	not used	56	1	Q1	BC849C	
-----								
22	3	C219,C236,C237	220n	57	12	RN1,RN4,RN29,RN35,RN36, RN37,RN39,RN40,RN41,RN42, RN45,RN46		4x10k
23	7	C206,C207,C232,C233,C244, C245,C246	33p	58	5	RN5,RN6,RN9,RN10,RN11		4x22R
-----								
25	4	D7,D8,D9,D10	SMAJ5.0CA	59	5	RN8,RN20,RN21,RN32,RN38		4x330R
26	2	D15,D16	BAR43A	60	15	RN2,RN3,RN7,RN12,RN13,RN14, RN15,RN16,RN17,RN19,RN28, RN30,RN31,RN33,RN34		4x47R
27	1	F1	RUE250 / 2,5A / 0,04R	61	9	RN18,RN22,RN23,RN24,RN25, RN26,RN27,RN43,RN44		4x0R_Jmpr
28	1	IC1	EPXA1-484	62	38	R1,R2,R3,R6,R10,R19,R20, R23,R27,R29,R30,R34,R35, R44,R45,R46,R47,R48,R50, R51,R52,R53,R57,R58,R60, R66,R68,R74,R76,R78,R79, R88,R89,R95,R111,R113, R133,R137		0R_Jmpr
29	1	IC2	AM29LV640D-TSSOP48	63	20	R5,R7,R8,R14,R36,R37,R38, R39,R55,R67,R69,R70,R71, R72,R75,R77,R82,R96,R102, R112		10k
30	1	IC3	MD2811-Dxx-V3	64	6	R9,R93,R94,R119,R120, R146		10R
31	1	IC4	AM26LV31C_SO16	65	6	R11,R12,R13,R31,R32,R106		4R7
32	1	IC5	MT48LC16M16_TSOP54	66	5	R15,R18,R24,R56,R103		3k3
33	1	IC6	AM26LV32C_SO16	67	2	R16,R17		not populated
34	1	IC7	TTCrx	68	9	R21,R25,R26,R54,R59,R81,		100R
35	1	IC8	TPS3306-18DGK					
36	1	IC9	LXT971ALC					
37	3	IC10,IC17,IC18	SN75LVDS391PW					
38	1	IC11	MIC39151-1.8BU					
39	1	IC12	MIC29301-3.3BU					
40	1	IC13	AD7708BRU					
41	1	IC14	LC4064ZC-75T48					
42	1	IC15	REG711EA-5					
43	1	IC16	NC7SZ86P5X					
44	2	IC19,IC20	SN75LVDT390PW					
45	1	IC21	AD1582ART					
46	1	IC22	AD8351ARM					
47	1	IC23	LC4032ZC-75T48					
48	1	IC24	QPLL					
49	1	IC25	SN65LVCP22PW					
50	1	IC26	LP3985IM5-2.5					
51	7	LED1,LED2,LED6,LED7,LED8, LED9,LED10	green_0603					
52	3	LED3,LED4,LED5	red_0603					
53	5	OC1,OC2,OC3,OC4,OC5	LTV357T					
54	1	OR1	HFBR-2316T					
55	1	OSC1	IQXO-71					

R83,R97,R147

69	1	R22	SBridge	
70	10	R28,R33,R61,R65,R73,R84, R85,R101,R121,R125	150R	
71	2	R41,R40		8R06
72	12	R42,R43,R64,R80,R86,R124, R140,R141,R144,R145,R148, R149	51R	
73	1	R49	22k1_1%	
74	6	R62,R63,R98,R118,R142, R143	2k2	
75	4	R91,R117,R126,R132	4k7	
76	1	R104	330R	
77	2	R138,R139	25R	

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78	1	TR1	Halo TG110-S050N2	
79	1	XTAL1	25MHz	
80	1	XTAL2	32kHz	
81	1	XTAL3	CC1F-T1A ??MHz	
82	1	XTAL4	??MHz	